Thin Silicon R&D for LC applications

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- Status report
- Hybrid Pixel Detectors for LC

TESLA TDR

- Pixel micro-vertex r=1.5 cm -6 cm (VTX)
- Time Projection Chamber (TPC) provides not only good $\Delta p/p$ but also excellent dE/dx
- Silicon tracker (SIT) in barrel (to improve $\Delta p/p$)
- Silicon disks (FTD) and forward chamber (FCH) provide tracking in the forward region

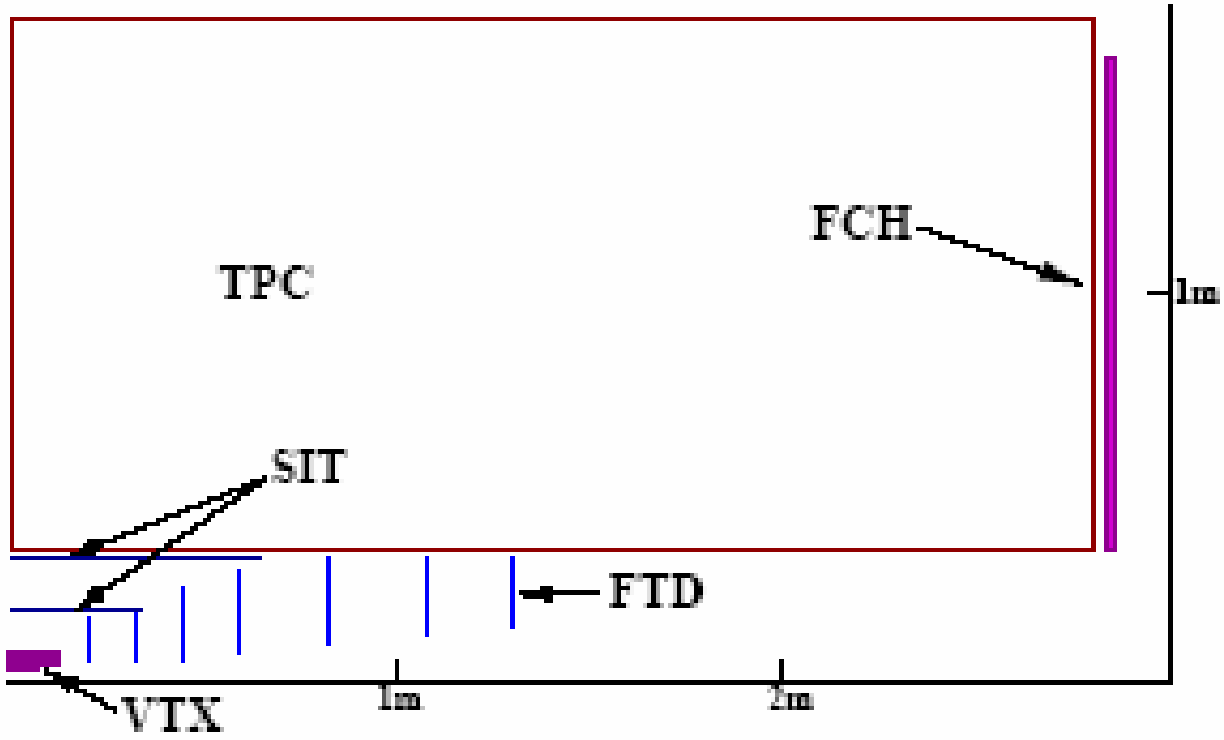
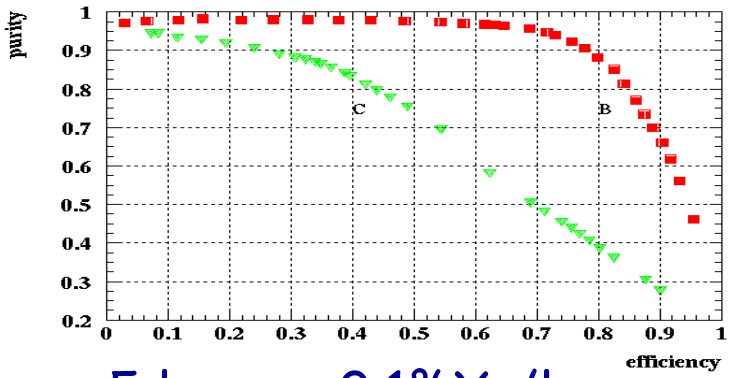


Figure 2.0.1: *General layout of the tracking system*

LC: Pixel Vertex Detector

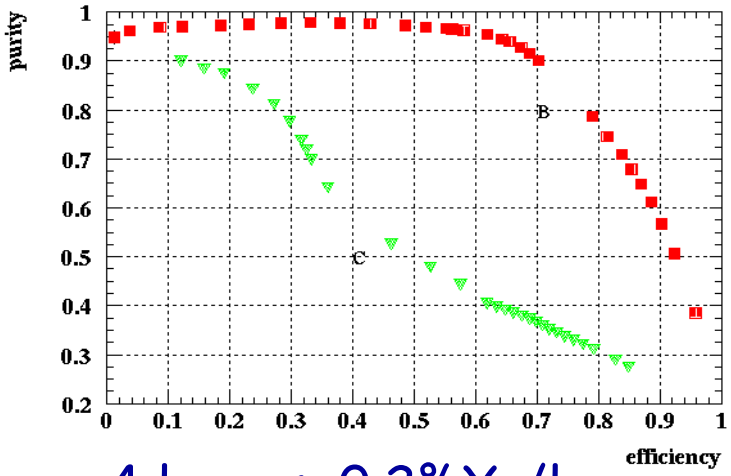
- CCD are the default option in the barrel
  - small pixel size ≅(20 μm)^2
  - excellent spatial resolution (<5 μm)
  - Slow readout (R&D)
  - Concern about radiation hardness (R&D)
  - Cooling
- DEPFET, MAPS

Stefania Xella



5 layers, 0.1%X_0/layer

Thinning SI bulk to 50 μm



4 layers, 0.2%X_0/layer

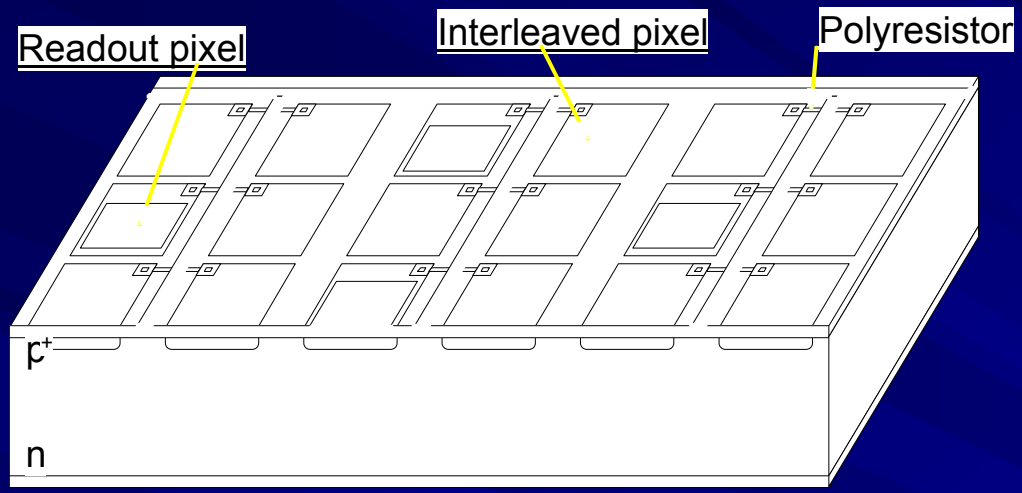
5 layers, 0.1%X_0

Thin Hybrid Pixels

- Hybrid Active Pixels
  - Advantages:
    - fast time stamping
    - sparse data read out
    - excellent radiation tolerance.
  - Further improvements are needed for:
    - point resolution, which is currently limited by the pixel dimensions of 50 μm $\times$ 300 μm limited by the VLSI. Can be improved by using interleaved pixel cells which induce a signal on capacitively coupled read-out pixels
    - reduction in material (thin silicon)
  - Interesting for the FTD ???
- Purdue is collaborating with J. Fast, S. Kwan, W. Wester and C. Gingu at Fermilab on LC effort. Proposal was submitted to the NSF.

Interleaved pixels

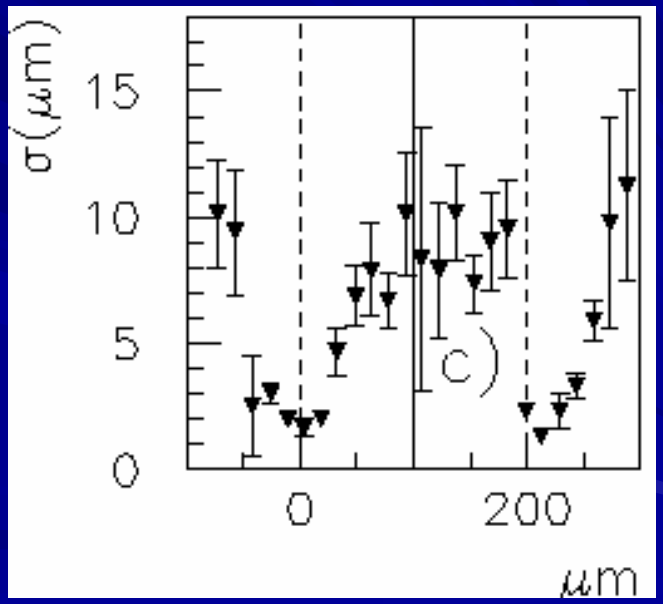
- Work has been done by Caccia, Bataglia, Niemiec et al.



readout pitch = n x pixel pitch

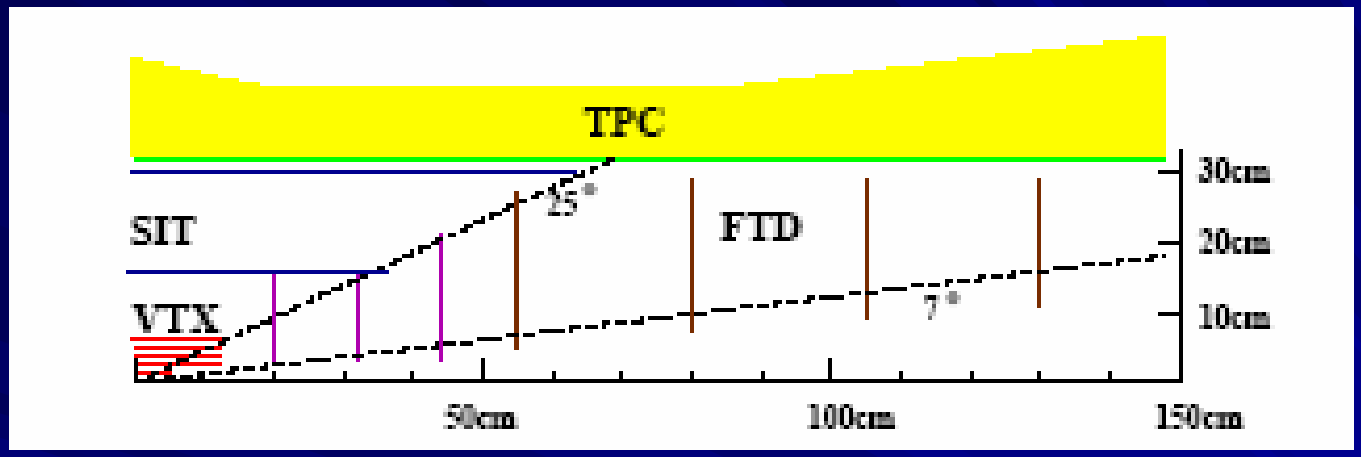
Large enough to house the VLSI front-end cell

Small enough for an effective sampling

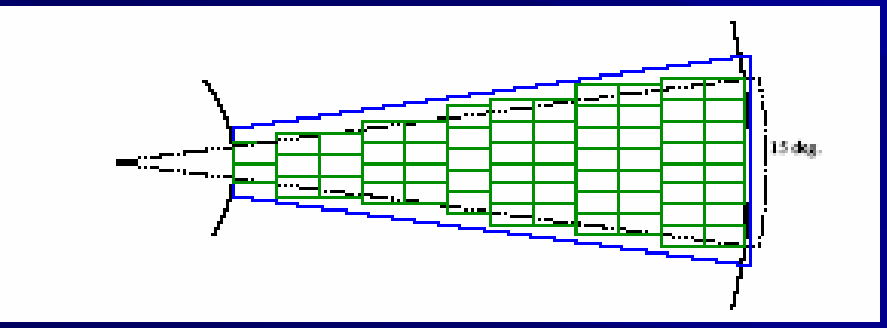


- Structures with: 60 μm implant width, 100 μm pixel pitch, 200 μm readout pitch yield resolution:
  - Interleaved pixels (max charge sharing): 3 μm
  - Readout pixels (min charge sharing): 10 μm
- New prototypes with Pixel pitch 25 μm x 25 μm and 25 μm x 50 μm should yield improved performance

TESLA: Forward tracking



- Layout of a forward pixel layer

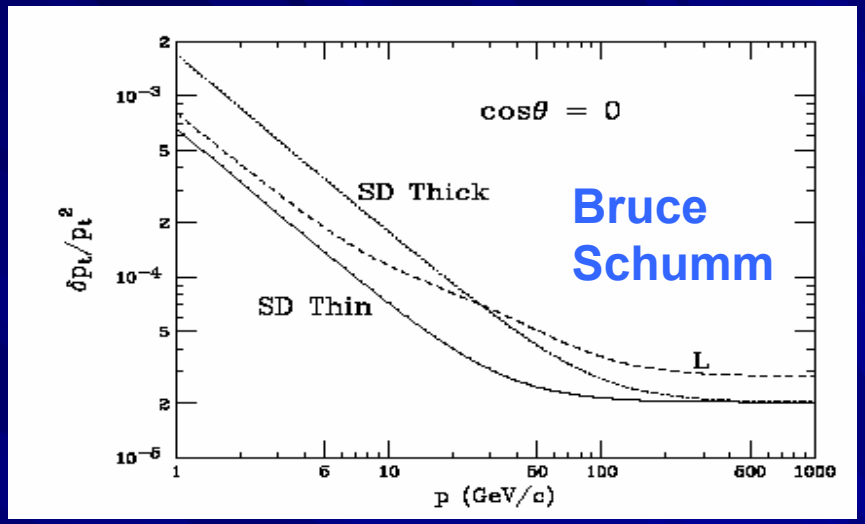


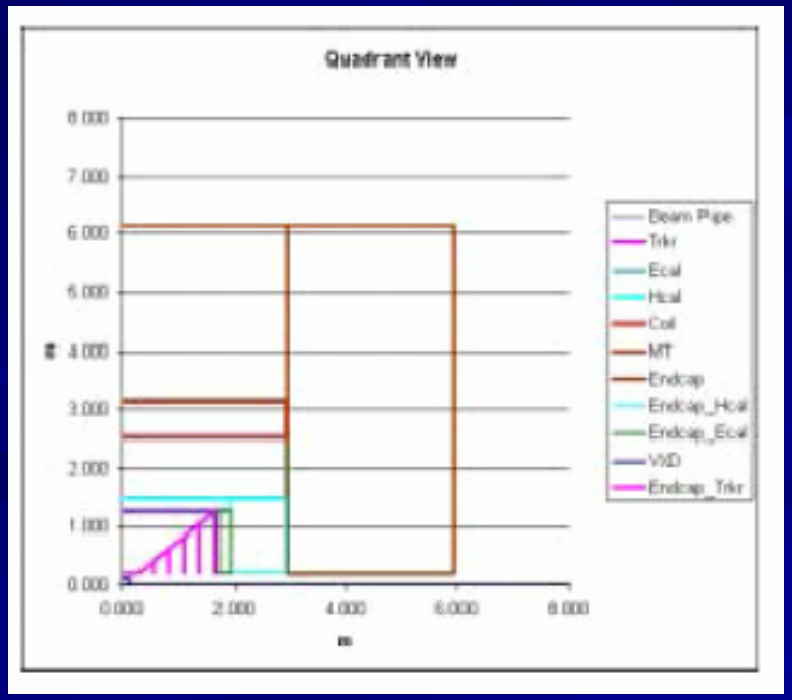
- Layout of a forward strip layer

- Material minimization is important

LC: tracking

- Gaseous detector (TPC-TESLA):
  - Large
  - many samplings/track
  - dE/dx





- Silicon option NLC:
  - Small
  - 5 samplings/track
  - No dE/dx
  - Reduce volume of Ecal (SiW)
- SD thin achieves good momentum resolution
  - 3 thin inner layers (200 μm)
  - 2 outer layers (300 μm)

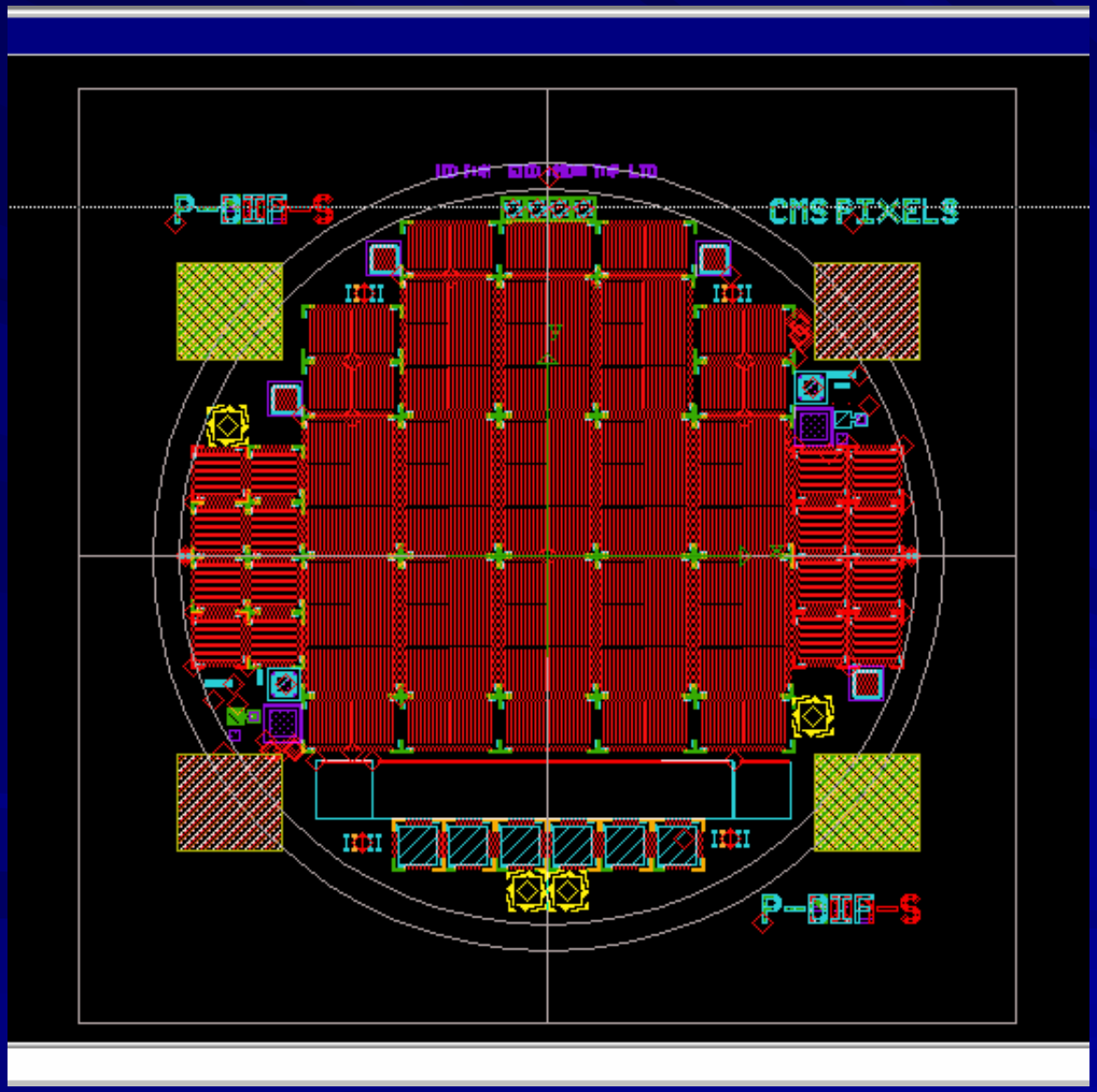
Thin silicon R&D at Purdue

- Technical problems:
  - Manufacturing of thin devices is difficult
  - Thinning after processing is difficult
  - Industry has expressed interest in thin silicon devices
  - Collaboration with vendors is critical
- How thin:
  - The m.i.p. signal from such a thin, 50μm, silicon sensor layer is only ~3500 e-h pairs.
- R&D at Purdue has started last year. We got quotes from two vendors: Sintef and Micron
- Sintef: minimum thickness 140 μm on 4 inch wafers
- Micron: 4" Thickness range from 20μm to 2000μm, 6" Thickness range from 100μm to 1000μm

Thin silicon R&D

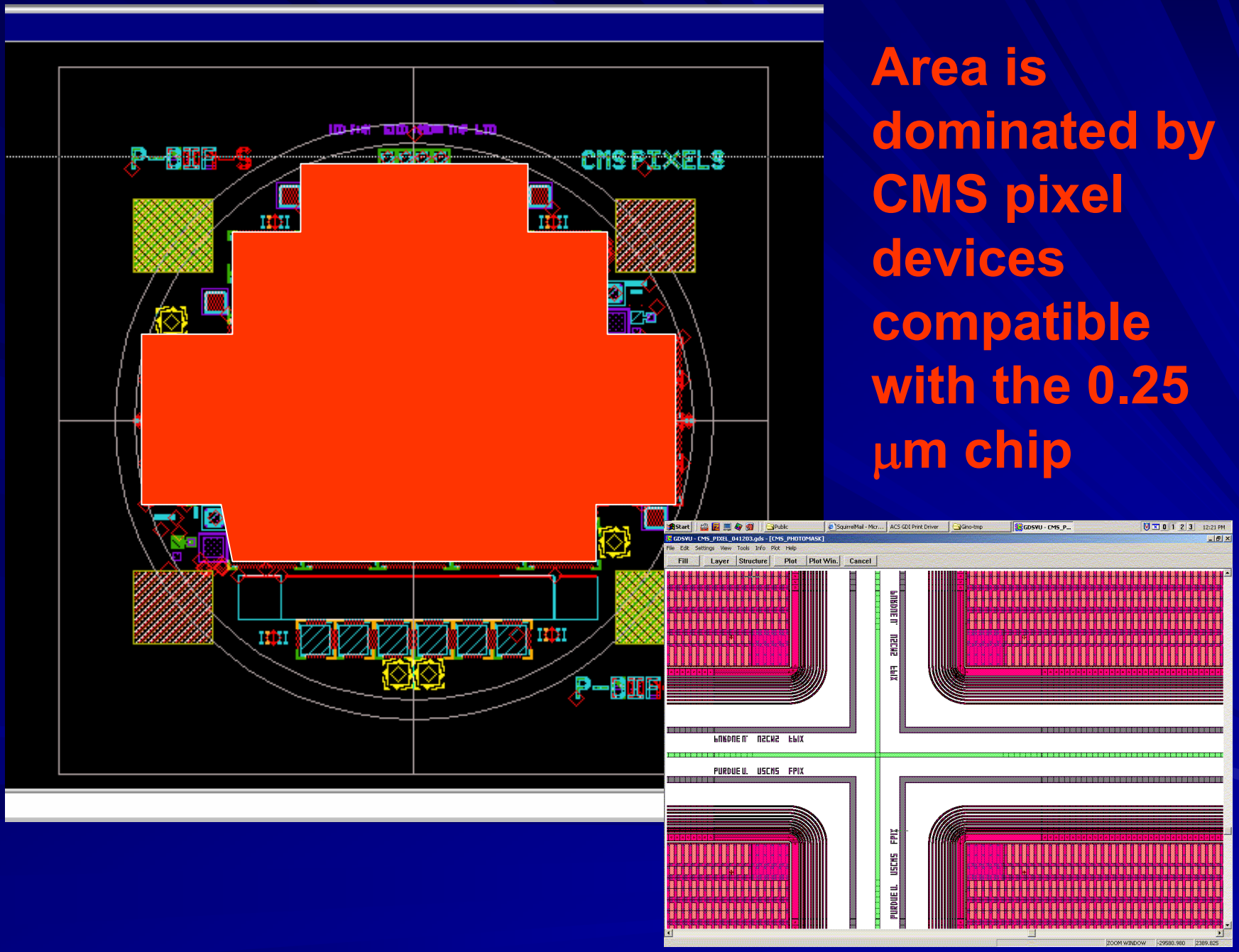
- We have selected Micron and we are exploring both n-on-n and p-on-n options.
- We expect to receive thin silicon strips sensors soon (fabricated with CDF-L00 masks)
- We will compare: 150, 200 and 300 μm thick strip detectors performance using the SVX4 chip developed for the so called "run 2b"
- Pixel masks have been designed. Each 6" wafer will contain:
  - Several pixels sensors matching the CMS $\frac{1}{4}$ micron chip (100 μm× 150 μm)
  - RD50 PAD structures for SLHC
  - Test structures to study bump bonding
- Sensors should be available for first tests in about 6 months.

Pixel Mask Layout

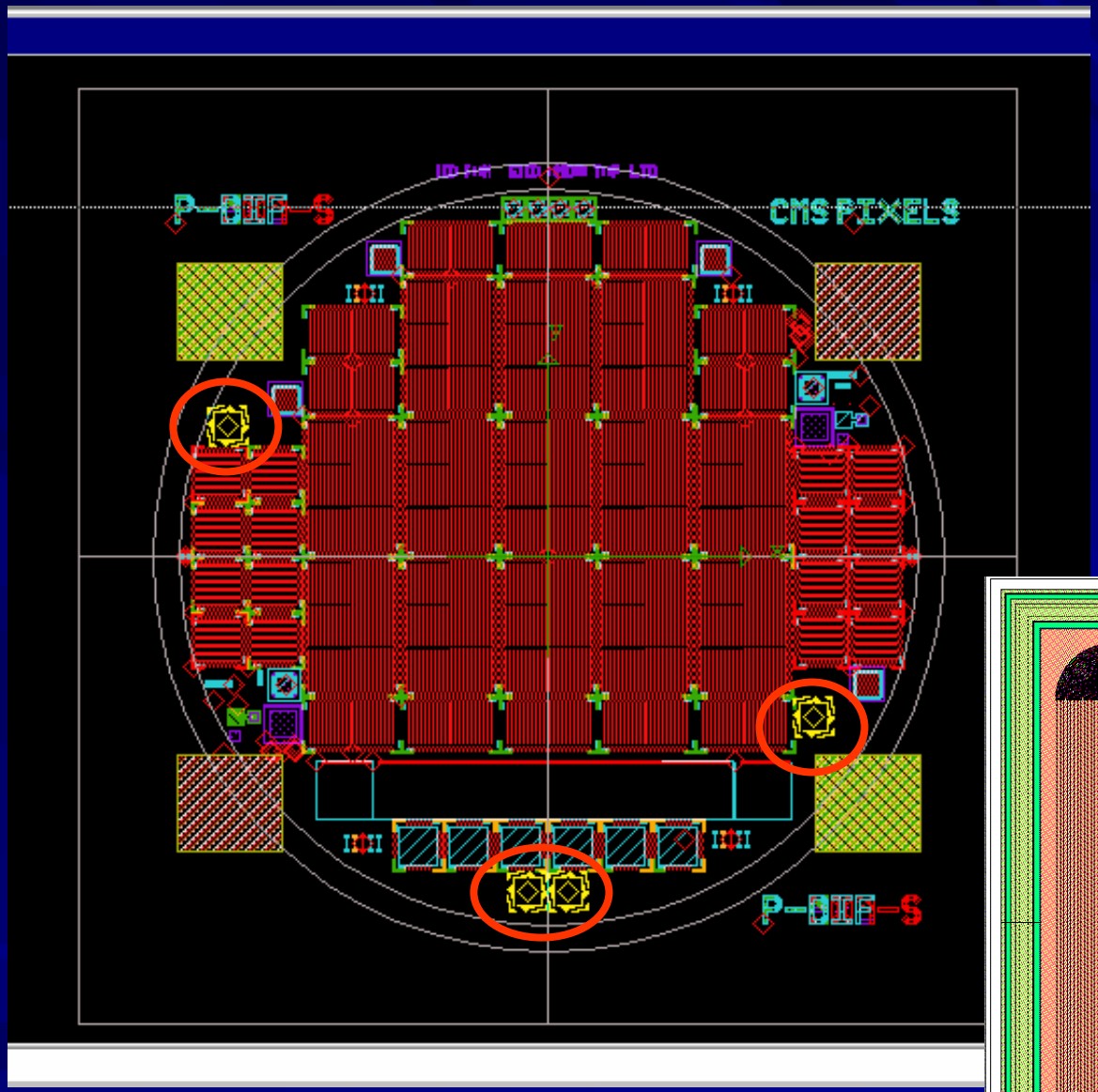


Masks (6”) are fabricated and processing (oxigenation) is starting this week.

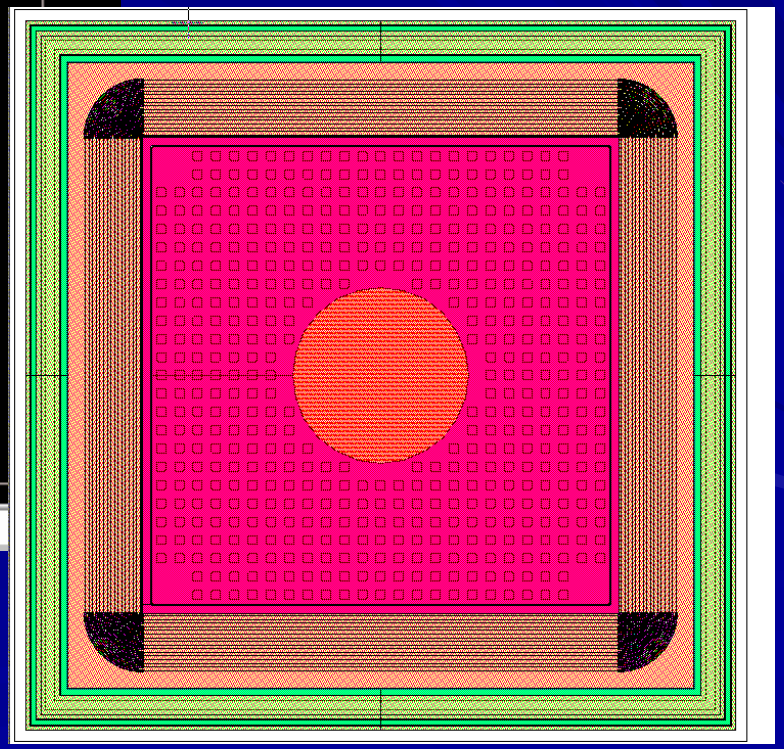
Devices out of fabrication within 3-4 months



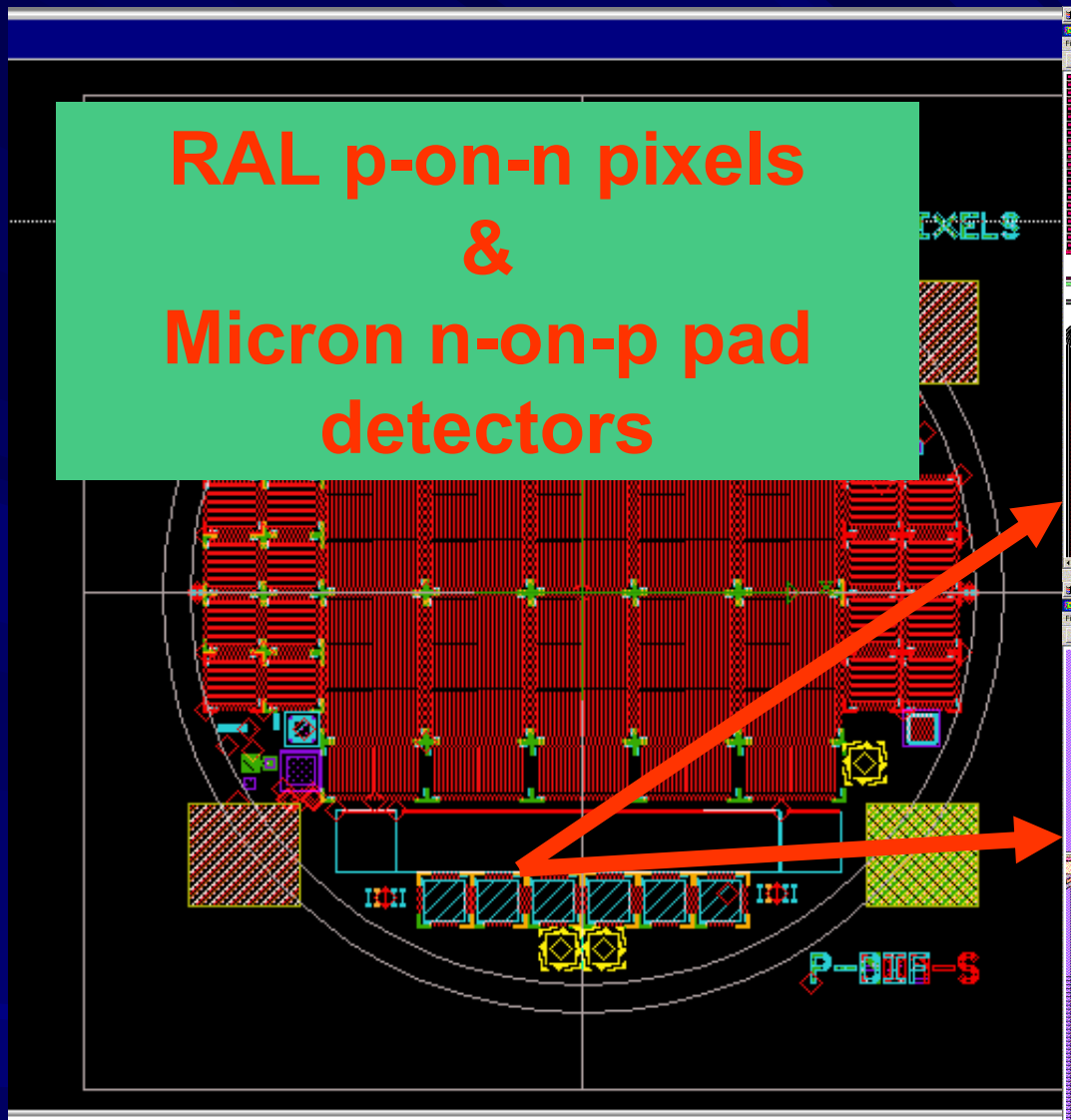
Area is dominated by CMS pixel devices compatible with the 0.25 μm chip

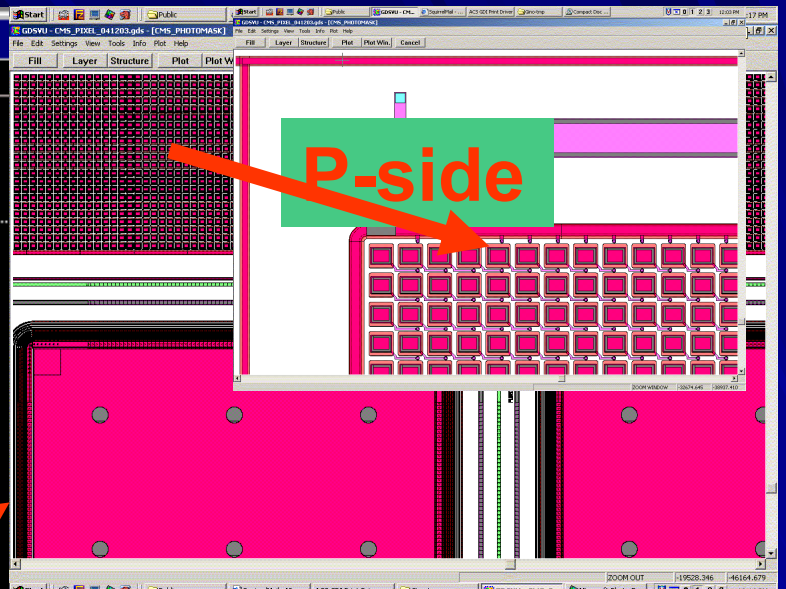


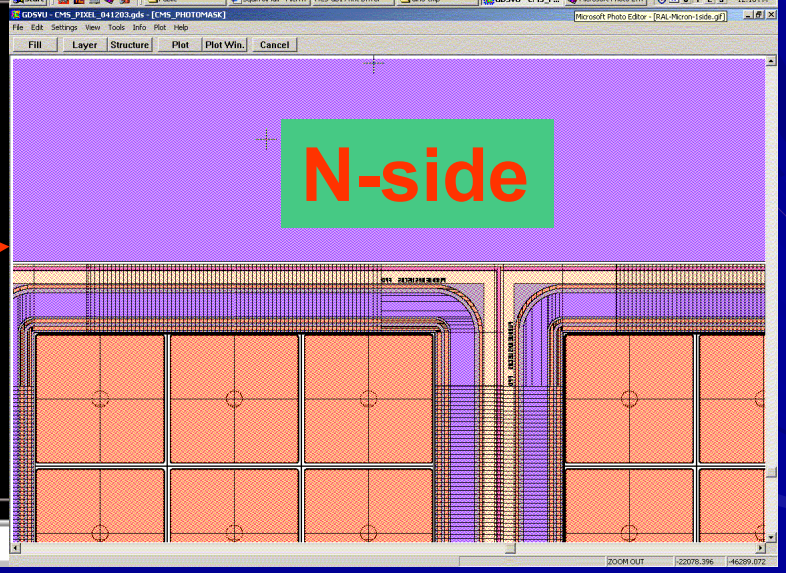
Circled in red the RD50 structures (diodes)



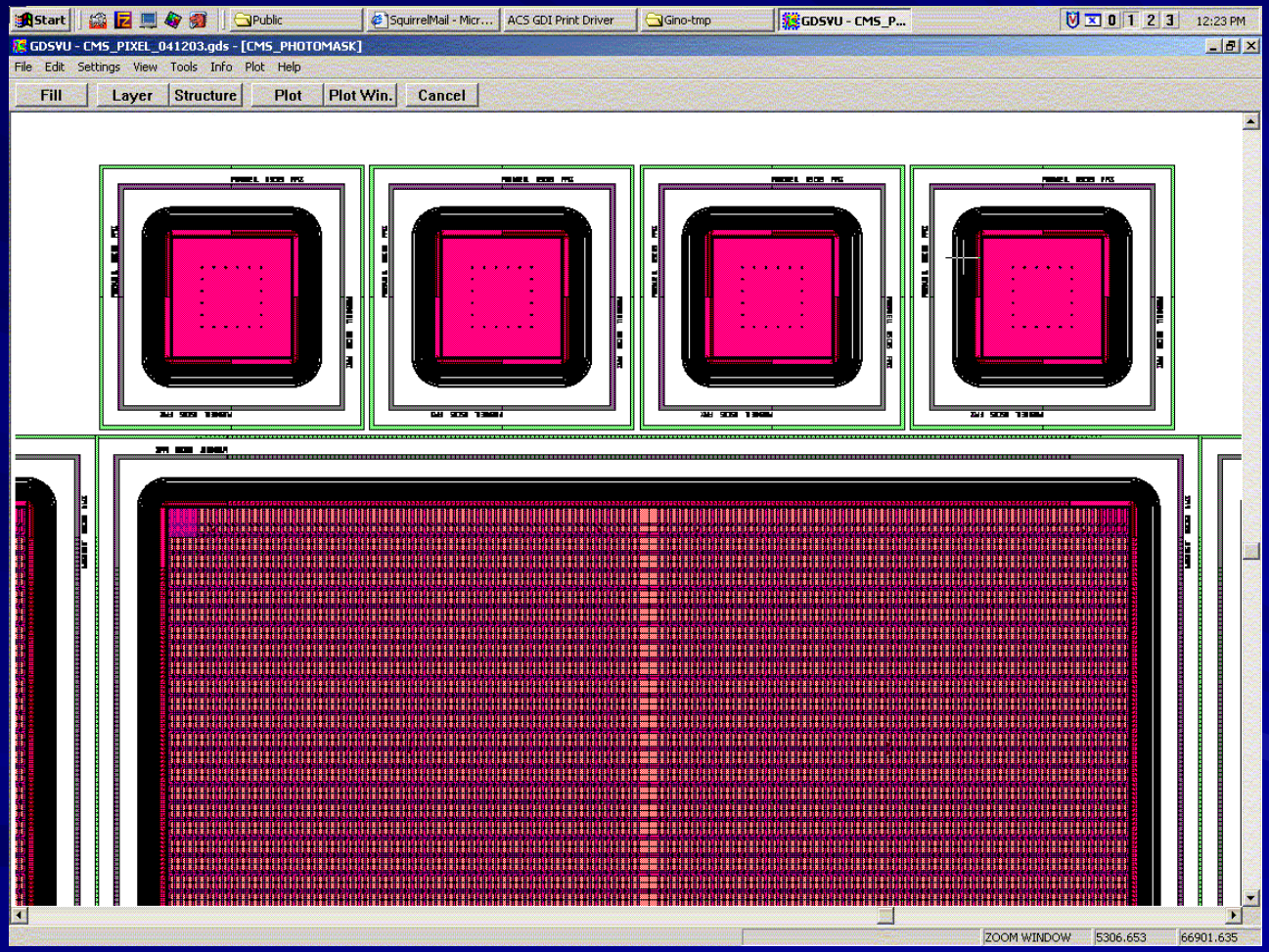
RAL p-on-n pixels & Micron n-on-p pad detectors





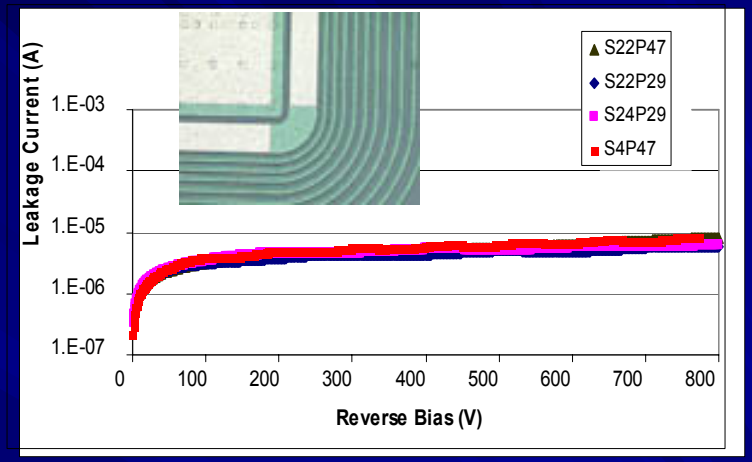


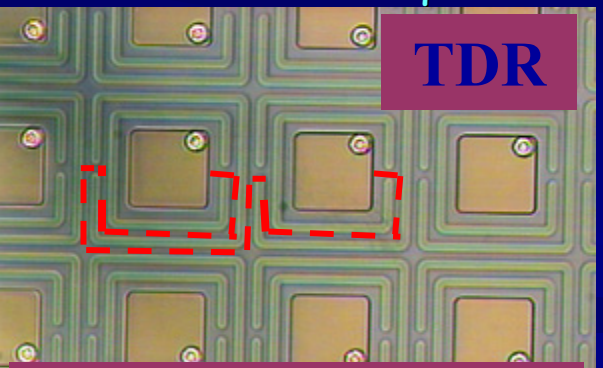
As usual diodes and other test structure for process control



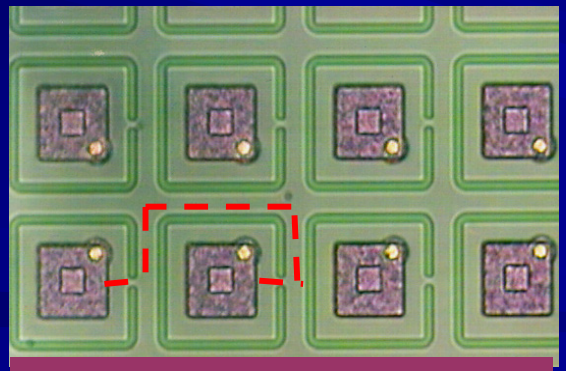
CMS Radiation Hard Design

- **Guard ring design:**
  - Limits lateral extension of the depletion region
  - Prevents breakdown at the device edge
  - 11 guard ring design implemented in SINTEF 1999 submission achieved NO BREAKDOWN up to >800 V after irradiation to ϕ = 6×10^{14} n_{eq}/cm^2





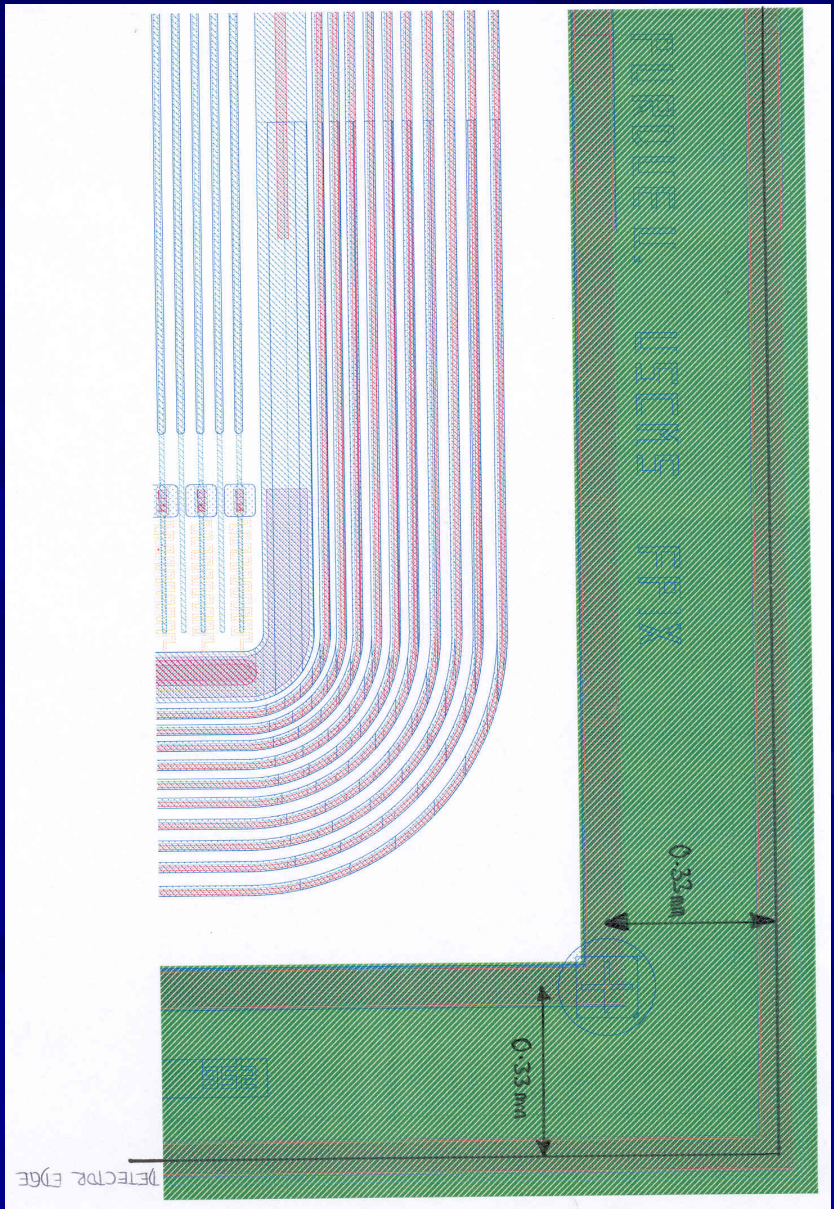
A : Double open ring



F: Single open ring

- **n^+-on-n option:**
  - Allows operation of un-depleted sensors after type inversion
  - N-side pixel isolation
    - P-stops (CMS)
  - SINTEF 1999 showed that F design was promising

Detail of a thin strip detector



Conclusions

- Material minimization for LC applications makes thin silicon development very interesting
- Thin silicon is also more rad-hard ⇒ Synergy between our LC interest and LHC commitments
- Several thin silicon strip and pixel sensors will be available to study:
  - Mechanical stability
  - Bump bonding feasibility
  - Readout and geometry not yet optimal for LC application
  - Simulation studies are needed to guide this effort and to provide input for future submissions and optimize geometry