Progress towards a Long Shaping-Time Readout for Silicon Strips

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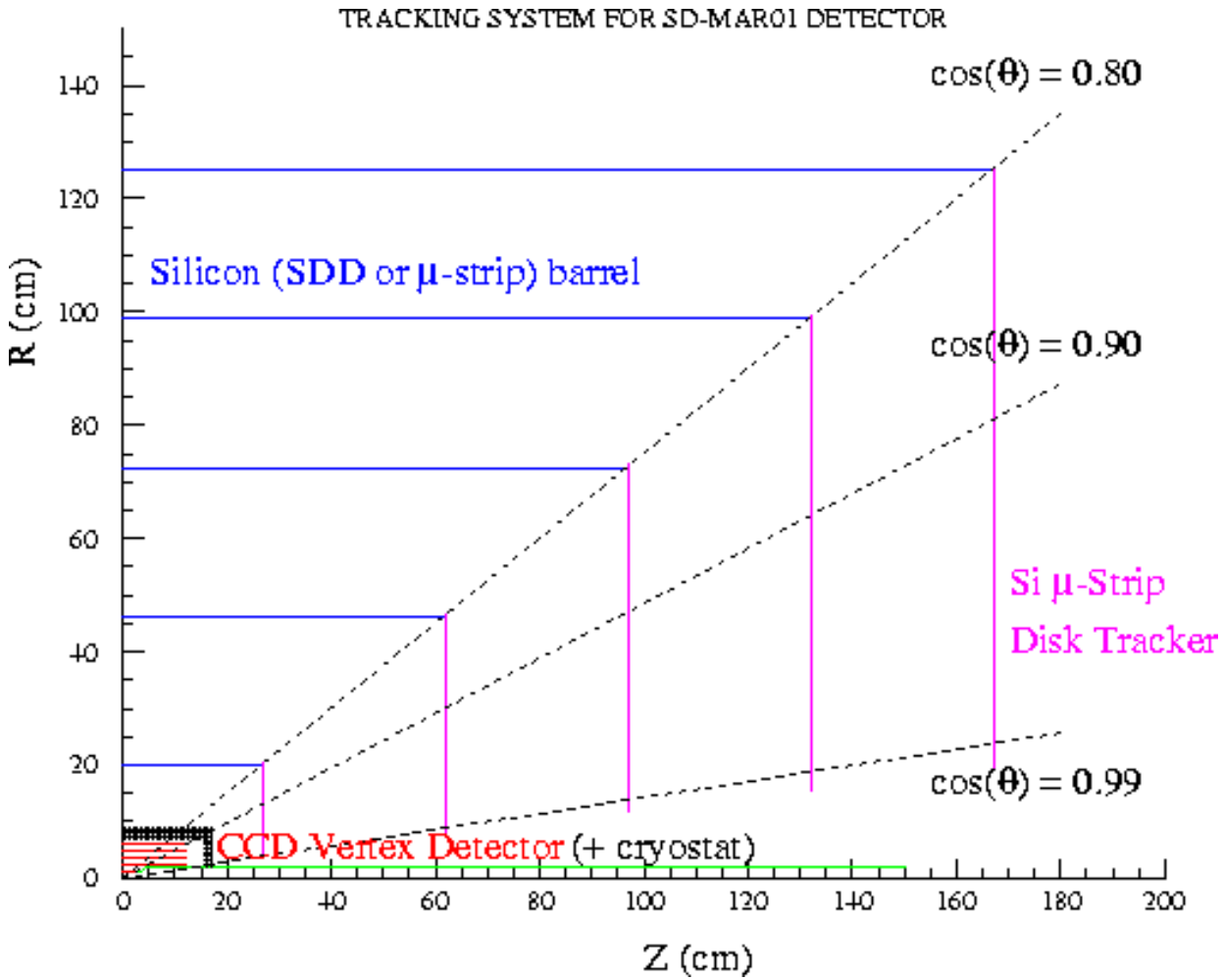
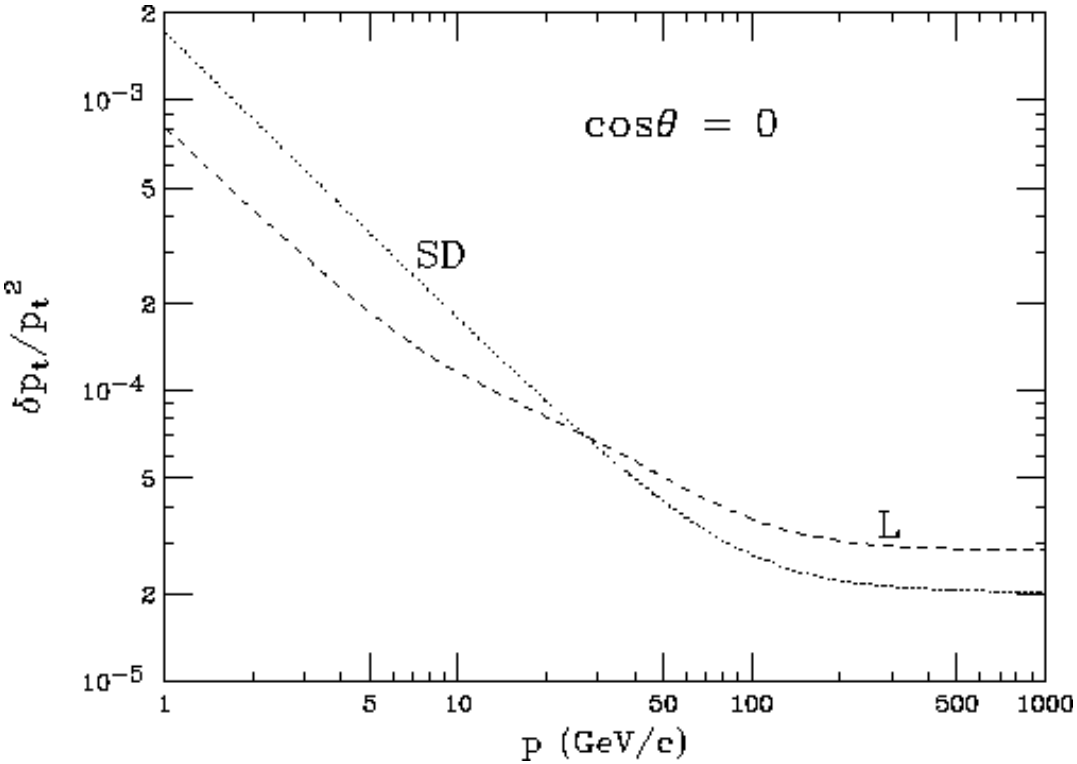
The SD Tracker



Tracker Performance



SD Detector burdened by material in five tracking layers (1.5% X_0 per layer) at low and intermediate momentum

Code: http://www.slac.stanford.edu/~schumm/lcdtrk.tar.gz

Idea: Noise vs. Shaping Time

Agilent 0.5 μm CMOS process (qualified by GLAST)

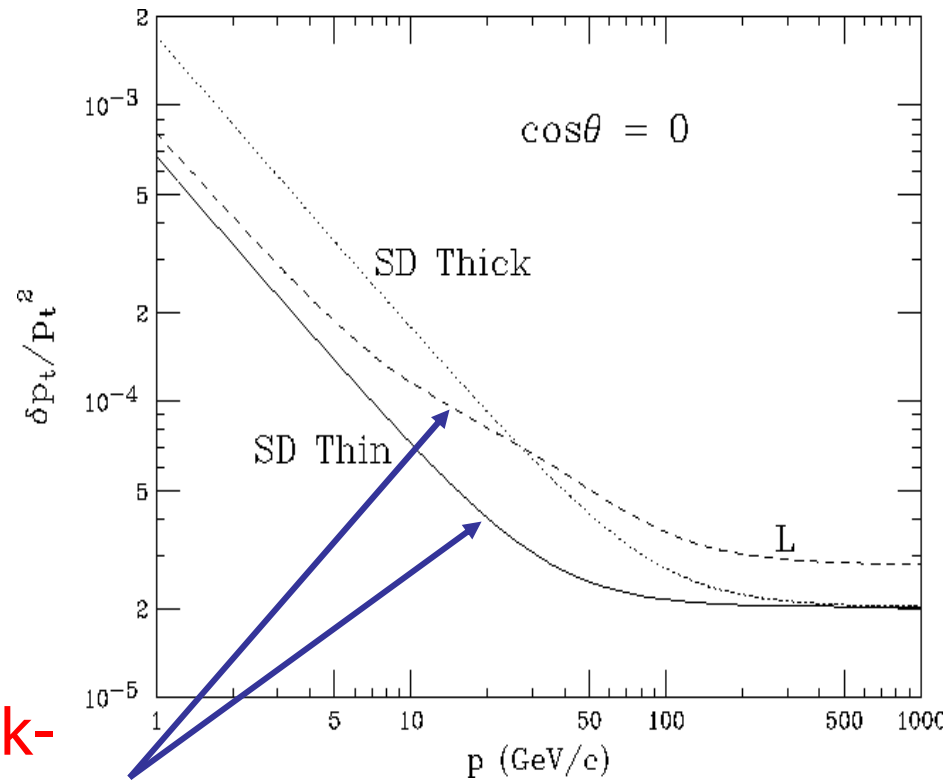
Min-i for 300μm Si is about 24,000 electrons

Shaping (μs)	Length (cm)	Noise (e^-)
1	100	2200
1	200	3950
3	100	1250
3	200	2200
10	100	1000
10	200	1850

The Gossamer Tracker

Ideas:

- Long ladders ➔ substantially limit electronics readout and associated support
- Thin inner detector layers
- Exploit duty cycle ➔ eliminate need for active cooling



➔ Competitive with gaseous tracking over full range of momenta

Also: forward region…

TPC Material Burden

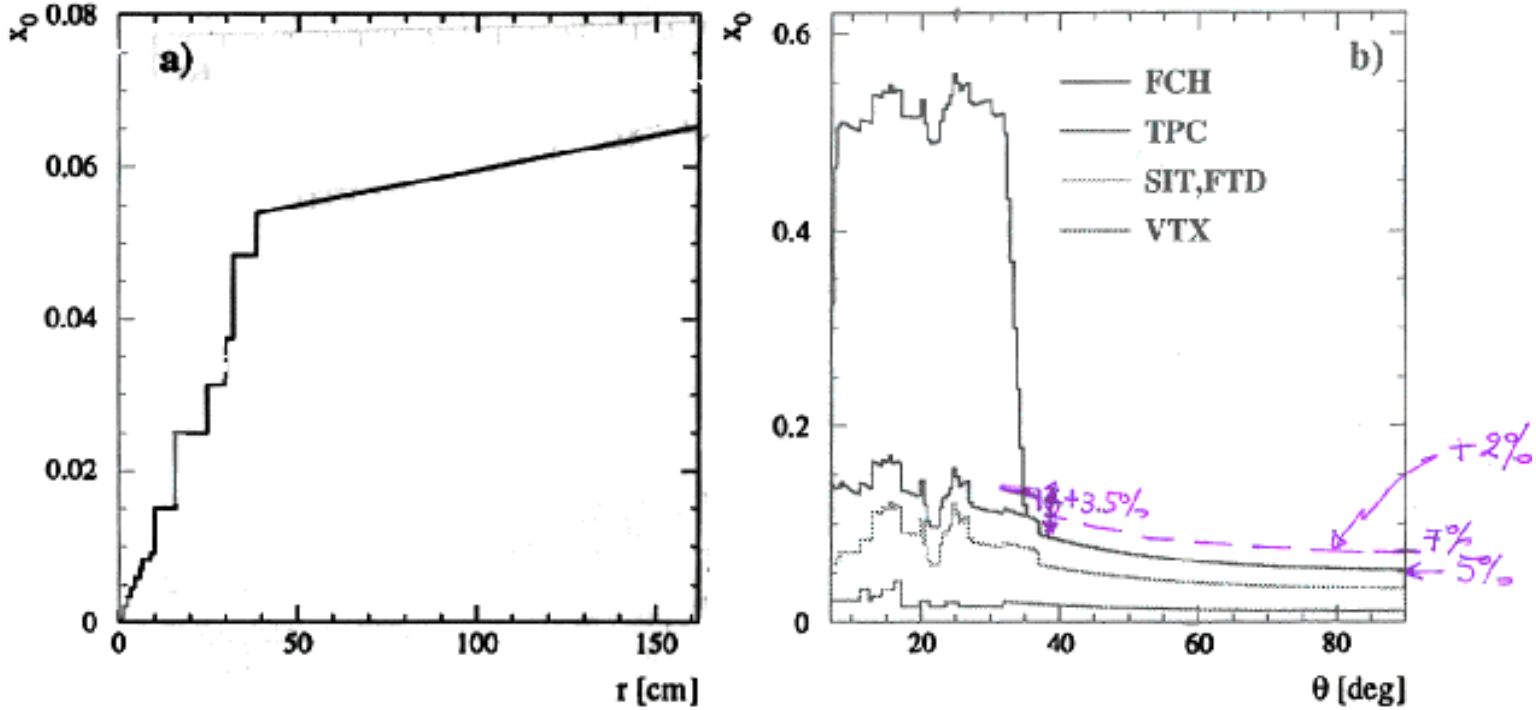


Figure 1.0.2: *Material distribution (a) as a function of the radius for $\theta = 90°$ and (b) as a function of the polar angle up to the end of the different subdetectors. For the line labelled TPC the material up to the end of the sensitive volume is shown.*

Pursuing the Long-Shaping Idea

LOCAL GROUP

SCIPP/UCSC

- Optimization of readout & sensors
- Design & production of prototype ASIC
- Development of prototype ladder; testing

➔ Supported by 2-year, $95K grant from DOE Advanced Detector R&D Program

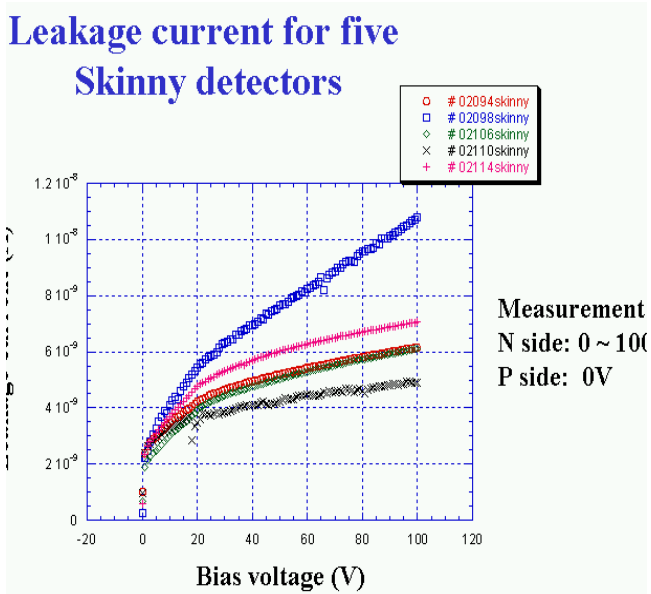
The SCIPP/UCSC Effort

Faculty/Senior	Post-Doc	Student
Alex Grillo Hartmut Sadrozinski Bruce Schumm Abe Seiden	Gavin Nesom Jurgen Kroseberg	Christian Flacco (will do BaBar thesis)

Engineer: Ned Spencer (on SCIPP base program)

SCIPP/UCSC Development Work

Characterize GLAST `cut-out' detectors (8 channels with pitch of ~200 μm) for prototype ladder

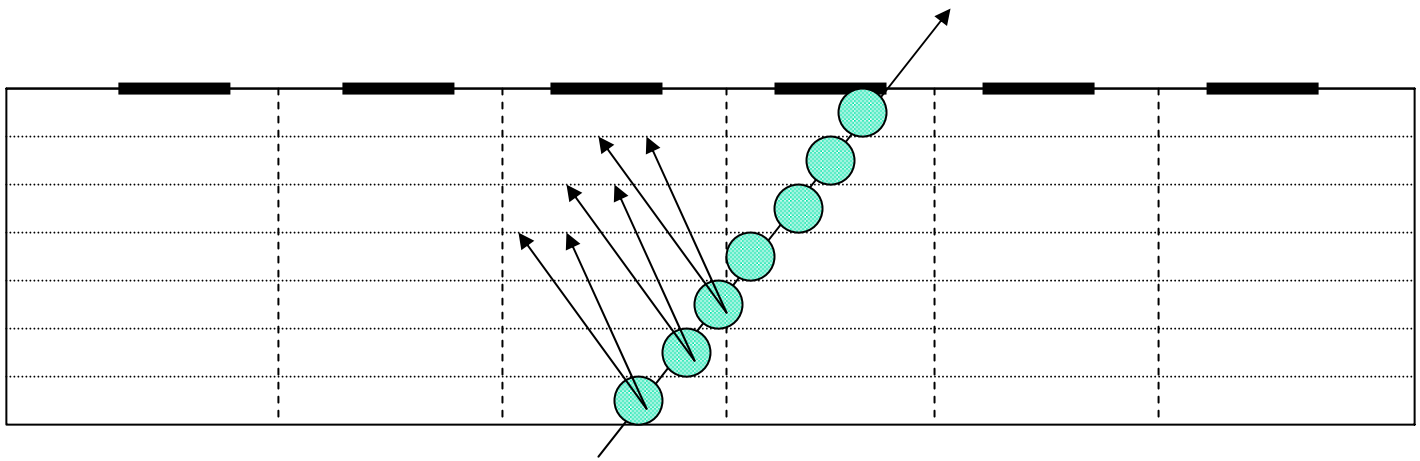


Detailed simulation of pulse development, electronics, and readout chain for optimization and to guide ASIC development (most of work so far)…

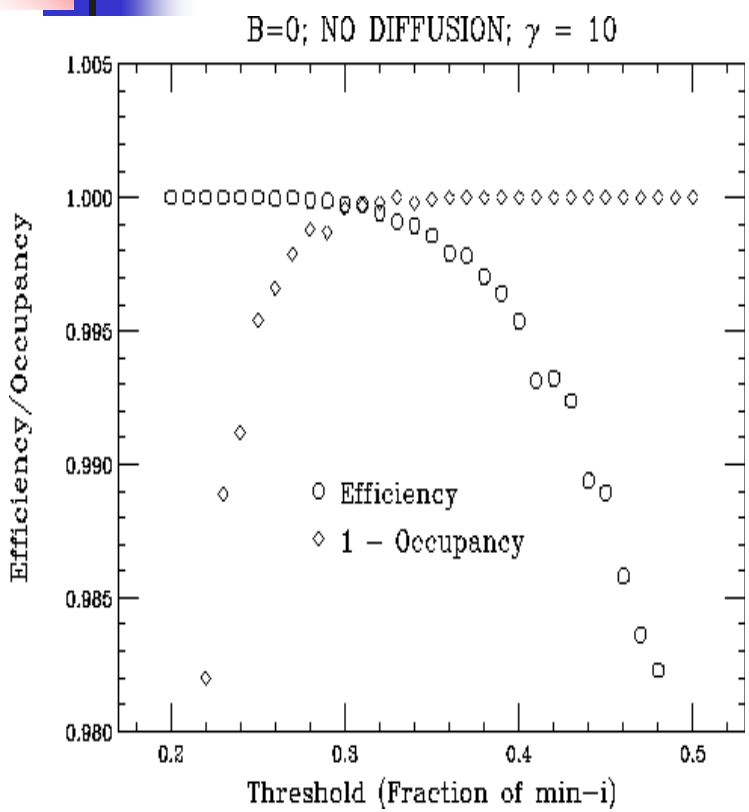
Pulse Development Simulation

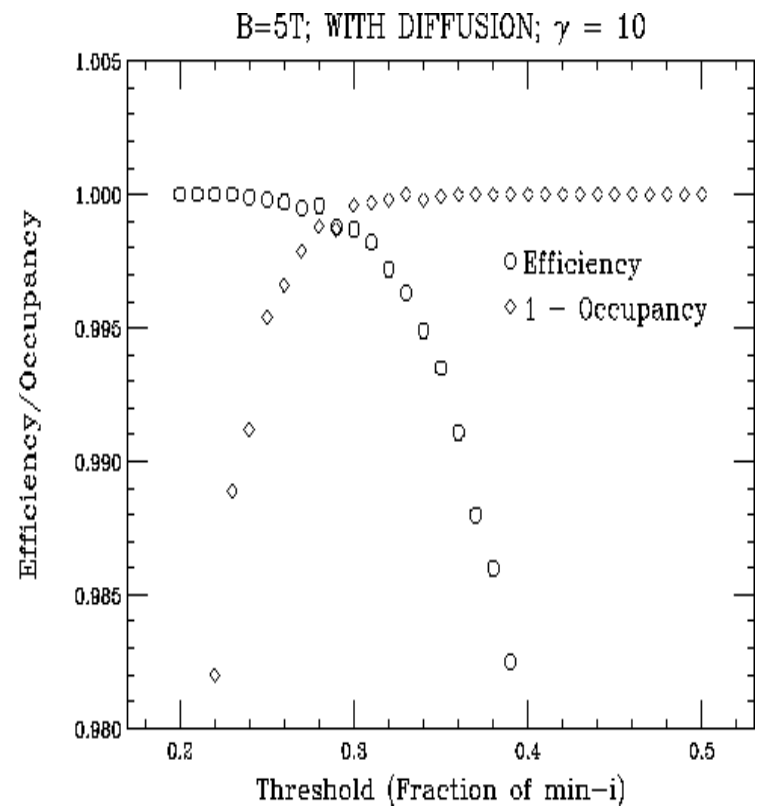
Long Shaping-Time Limit: strip sees signal if and only if hole is collected onto strip (no electrostatic coupling to neighboring strips)

Incorporates: Landau statistics (SSSimSide; Gerry Lynch LBNL), detector geometry and orientation, diffusion and space-charge, Lorentz angle, electronic response



Result: S/N for 167cm Ladder





At shaping time of 3μs; 0.5 μm process qualified by GLAST

Analog Readout Scheme: Time-Over Threshold (TOT)

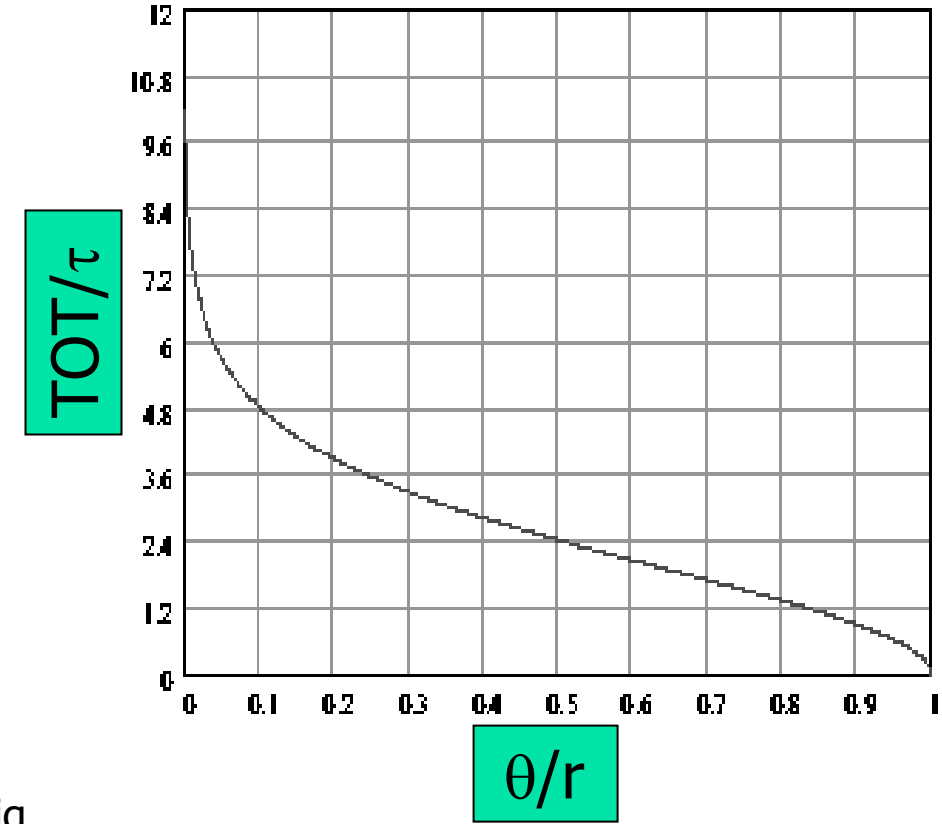
$$\theta = \frac{n_e^{\text{thresh}}}{< n_e >_{\text{min-i}}} \qquad r = \frac{n_e^{\text{pulse}}}{< n_e >_{\text{min-i}}}$$

TOT given by difference between two solutions to

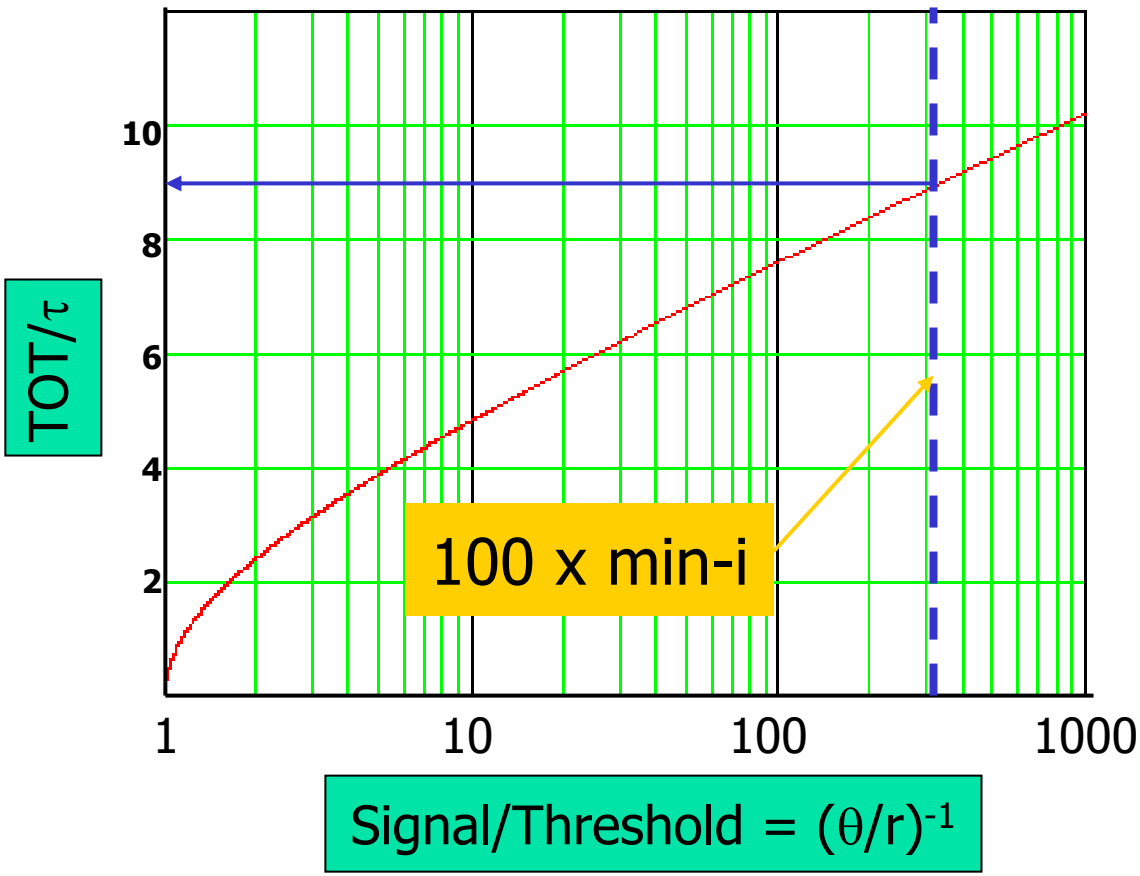
$$\frac{\theta}{r} = \frac{et}{\tau} e^{-t/\tau}$$

(RC-CR shaper)

Digitize with granularity τ/n_{dig}



Why Time-Over-Threshold?



With TOT analog readout:

Live-time for 100x dynamic range is about 9τ

With τ = 3 μs, this leads to a live-time of about 30 μs, and a duty cycle of about 1/250

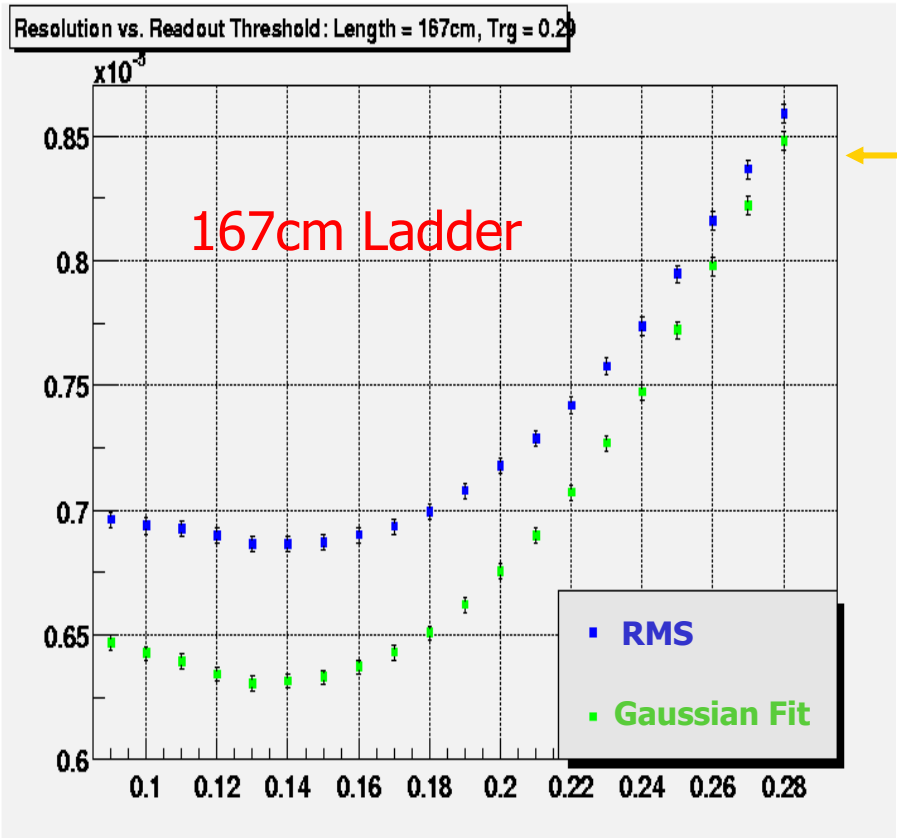
➔ Sufficient for power-cycling!

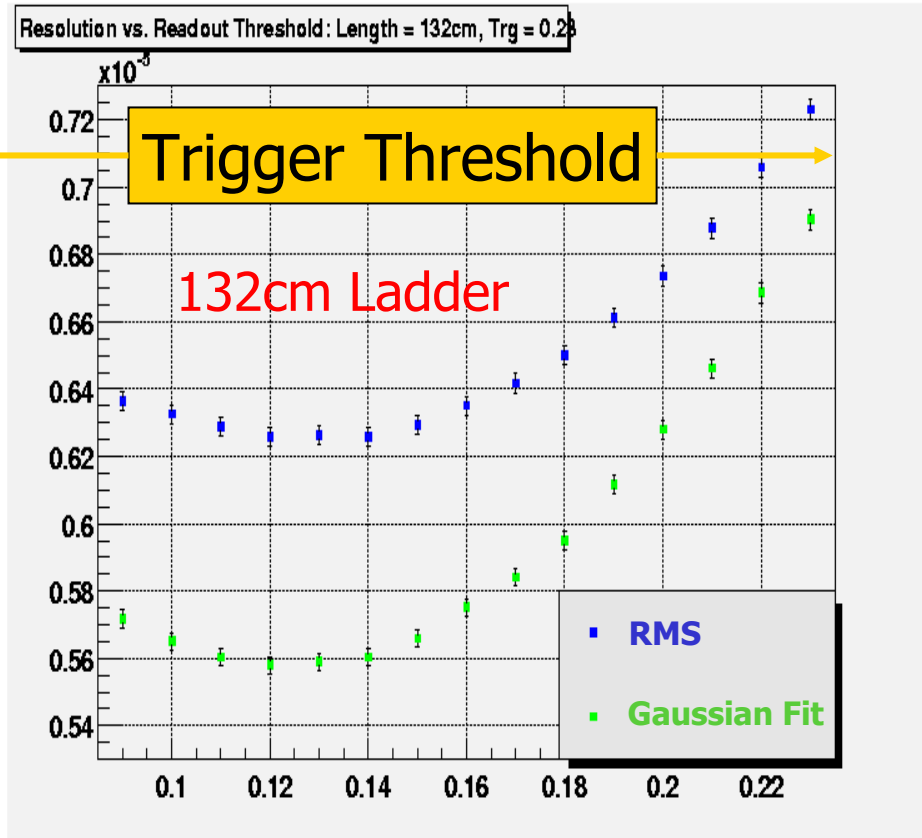
Single-Hit Resolution

Design performance assumes 7μm single-hit resolution. What can we really expect?

- Implement nearest-neighbor clustering algorithm
- Digitize time-over-threshold response (0.1*τ more than adequate to avoid degradation)
- Explore use of second `readout threshold' that is set lower than `triggering threshold'; major design implication

Resolution With and Without Second (Readout) Threshold





Readout Threshold (Fraction of min-i)

Lifestyle Choices

Based on simulation results, ASIC design will incorporate:

- 3 μs shaping-time for preamplifier
- Time-over-threshold analog treatment
- Dual-discriminator architecture

The design of this ASIC is now underway.

Challenges

Cycling power quickly is major design challenge

Warm machine: At 120 Hz, must conduct business in ~150 μs to achieve 98% power reduction

What happens when amplifier is switched off?

- Drift of ~10 mV (or 1 fC in terms of charge) enough to fake signal when amp switched back on
- Challenging for circuit design (`matching')

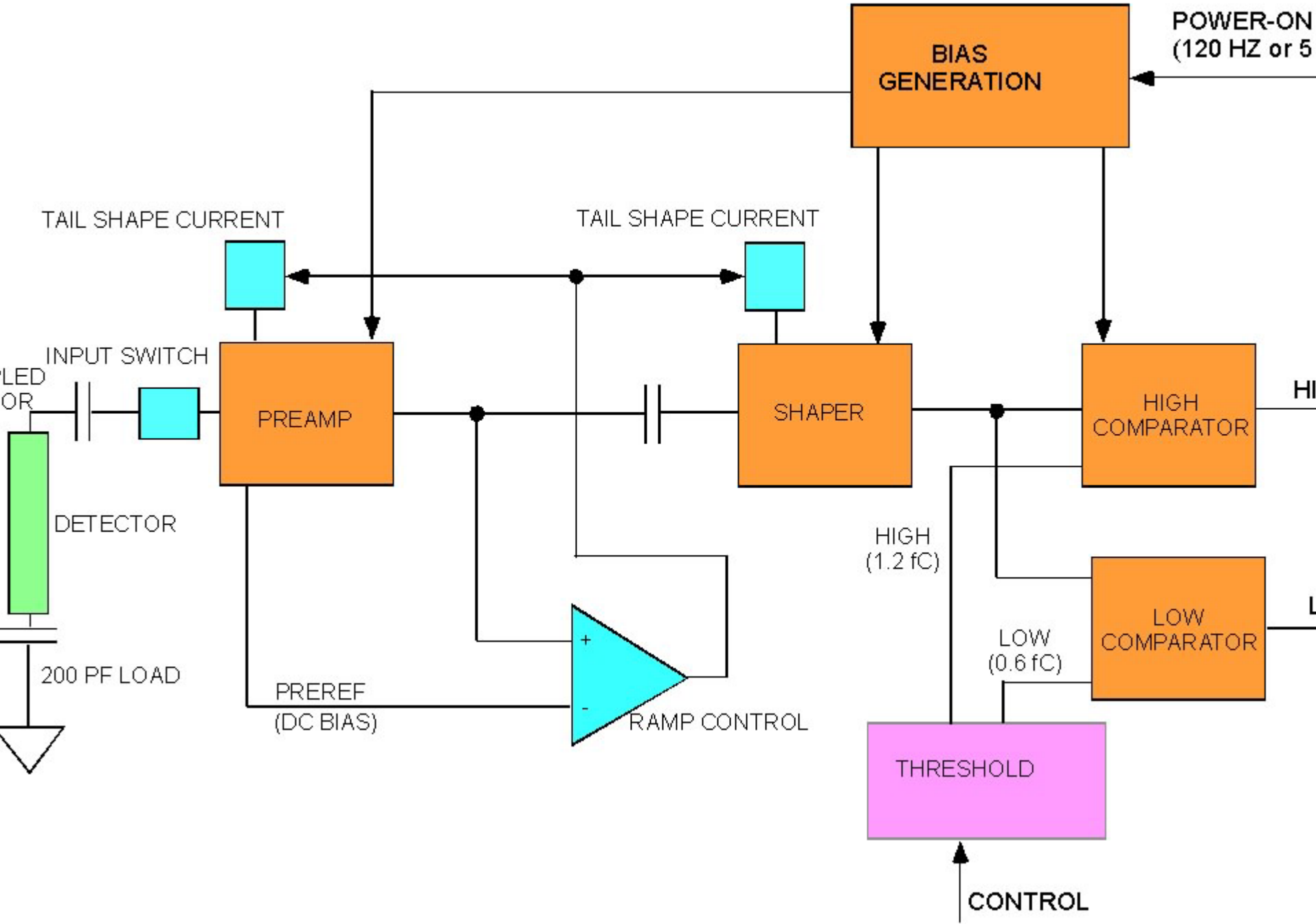
More Challenges

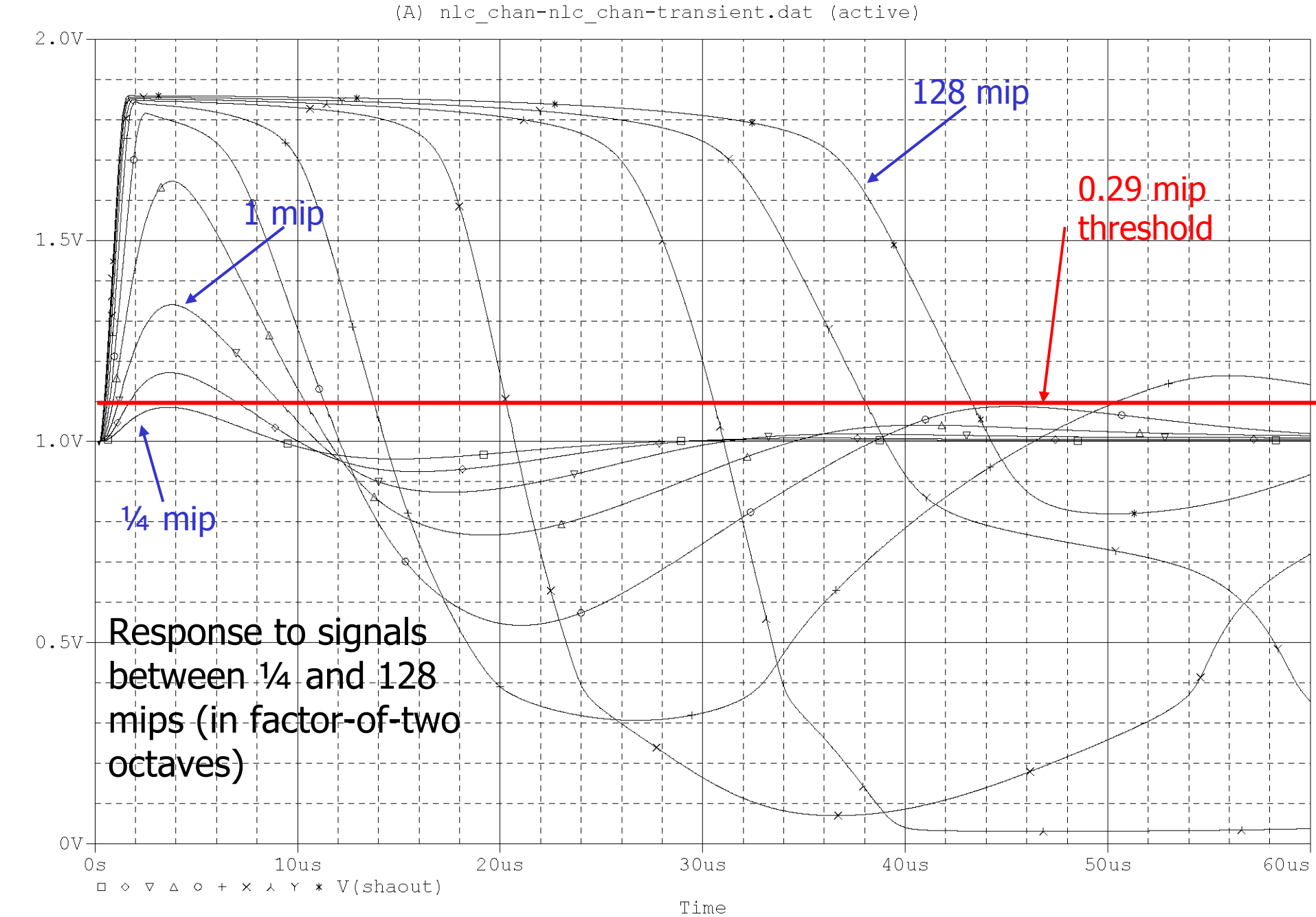
Trying to reach dynamic range of >100 MIP to allow for dEdX measurement of exotic heavy particles

At comparitor, MIP is about 500 mV, rail is about 1V

➔ Active `Ramp Control' forces current back against signal for few MIP and greater.

SILICON TRACKER FRONT-END ARCHITECTURE




(A) nlc_chan-nlc_chan-transient.dat (active)
2.0V
1.5V
1.0V
0.5V
0V
0s
10us
20us
30us
40us
50us
60us
Time
V(shaout)
128 mip
1 mip
¼ mip
0.29 mip threshold
Response to signals between ¼ and 128 mips (in factor-of-two octaves)

** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim
Date/Time run: 01/02/04 14:37:57 Temperature:

A1:(0.000,1.0002) A2:(559.875u,1.0038) DIFF(A):(-559.875u,-3.6378m)

Looking ahead

Challenges continue to arise in circuit design (but at least they're being caught before the chip is made!)

Layout in specific technology (0.25 μm mixed-signal RF process from Taiwan Semiconductor) lies ahead; substantial experience at SLAC and within UCSC School of Engineering ➔ Submit in March?

Long ladder, Nd:YAG pulsing system, readout under development

Project is very challenging, but progress is being made, albeit slower than first envisioned.