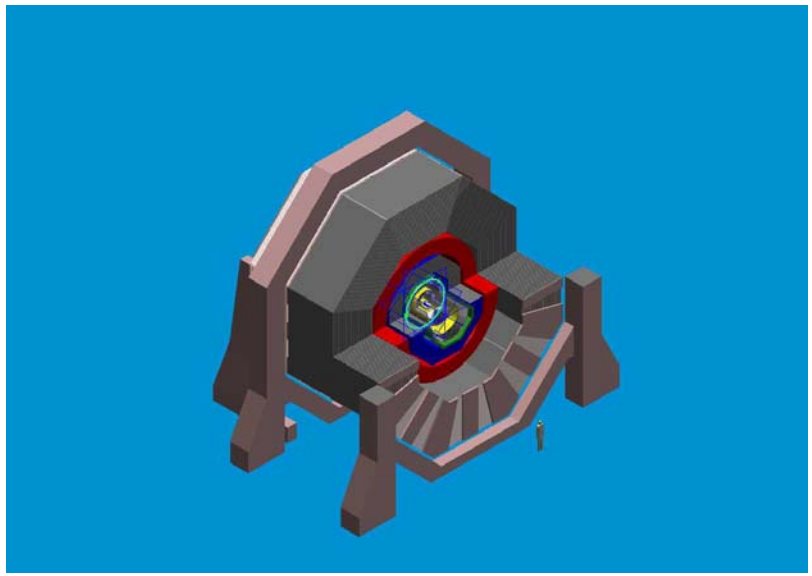
The Silicon Detector for the LC

- SiD = Silicon Detector
  - Motivation
  - Simulation
  - Technical efforts
  - L, E, P Measurement*
  - Status



* Not limited to SiD

SiD Motivation

- SiD is an attempt to interest the US HEP community, and the international community, in the experimental challenges of a LC.
- SiD represents an attempt to design a comprehensive LC detector, aggressive in performance but constrained in cost, that is also a "response" to the TESLA detector.
- SiD attempts to optimize the integrated physics performance capabilities of its subsystems.
- SiD might be considered a first step towards being one of the two detectors at the LC, but its development is substantially behind TESLA.
- SiD addresses warm technology advantages and challenges – but could handle cold.
- The design study should evolve the present concept of SiD towards a more complete and optimized design.

Nominal SiD Detector Requirements

- a) Two-jet mass resolution comparable to the natural widths of W and Z for an unambiguous identification of the final states.
- b) Excellent flavor-tagging efficiency and purity (for both b- and c-quarks, and hopefully also for s-quarks).
- c) Momentum resolution capable of reconstructing the recoil-mass to di-muons in Higgs-strahlung with resolution better than beam-energy spread .
- d) Hermeticity (both crack-less and coverage to very forward angles) to precisely determine the missing momentum.
- e) Timing resolution capable of tagging bunch-crossings to suppress backgrounds in calorimeter and tracker.
- f) Very forward calorimetry that resolves each bunch in the train for veto capability.

Detector Simulation Group

- Core LCD software development
  - R. Cassell, N. Graf, A. Johnson, J. McCormick*
- Additional SLAC manpower
  - T. Barklow, T. Maruyama, S. Wagner
  - M. Asai, W. Langeveld, D. Wright (SCS)
- Others @ SLAC
  - T. Abe, N. Sinev

Detector Response Simulation

- Using Geant4 to model detector physics.
- Flexible software framework to study performance as a function of detector parameters – e.g. R_{cal}, magnetic field, etc.
- Implementing realistic geometries, support material, readout technologies.
- Improving simulation of detector readout
  - digitization, merged hits, "ghost" hits, eff's

Detector Response Simulation II

- Whole-Detector approach emphasizes integrated "Particle Flow" reconstruction.
  - Parameterized fast MC indicates design requirements achievable.
  - Working to demonstrate with full *ab initio* reconstruction
    - Track finding & fitting + calorimeter cluster reconstruction from realistic detector hits in the presence of *full physics, detector, and machine backgrounds.*

International Collaboration

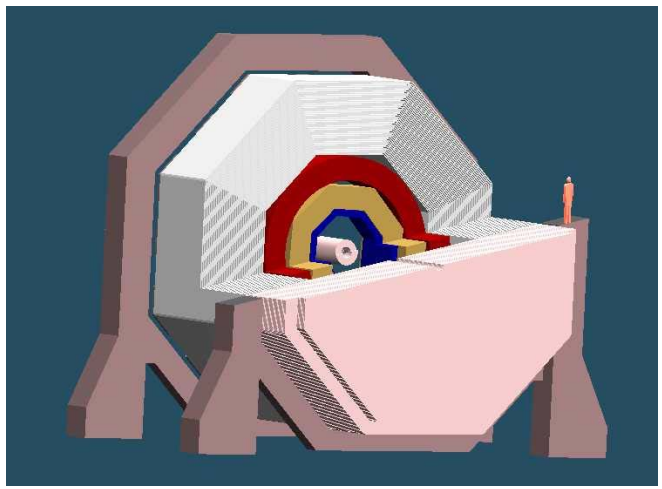
- LC Simulation community has standardized on common MC data content and I/O format.
  - American & ECFA groups already writing out and developing reconstruction/analysis code targeting LCIO
  - GLC simulations adopting xml for detector description & LCIO for simulation output to use in their framework.
- Active development of common reconstruction environment.
  - Allows code sharing & direct reconstruction comparison.
- Generation and sharing of data sets
  - Full SM physics backgrounds incl. $\gamma\gamma \rightarrow$hadrons.

Simulation Status & Short-term Goals

- Group is too small to simultaneously develop, maintain and undertake serious design studies of multiple detector proposals.
- Involving outside groups in core development.
- Concentrate on SiD, demonstrating tracker and EMCal performance.

SiD (Silicon Detector)

- Conceived as a high performance detector for NLC
- Reasonably uncompromised performance
  But
- Constrained & Rational cost
  - Detectors will get about 10%
  - of the LC budget: 2 detectors,
  - so $350 M each

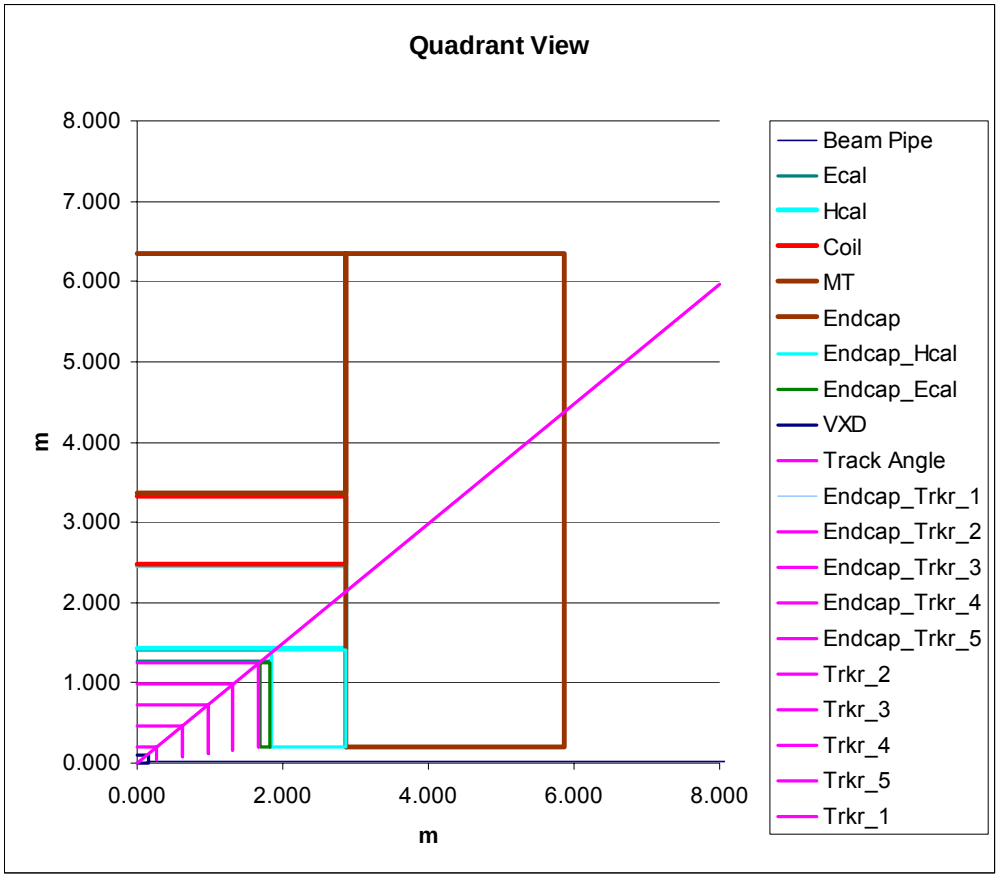


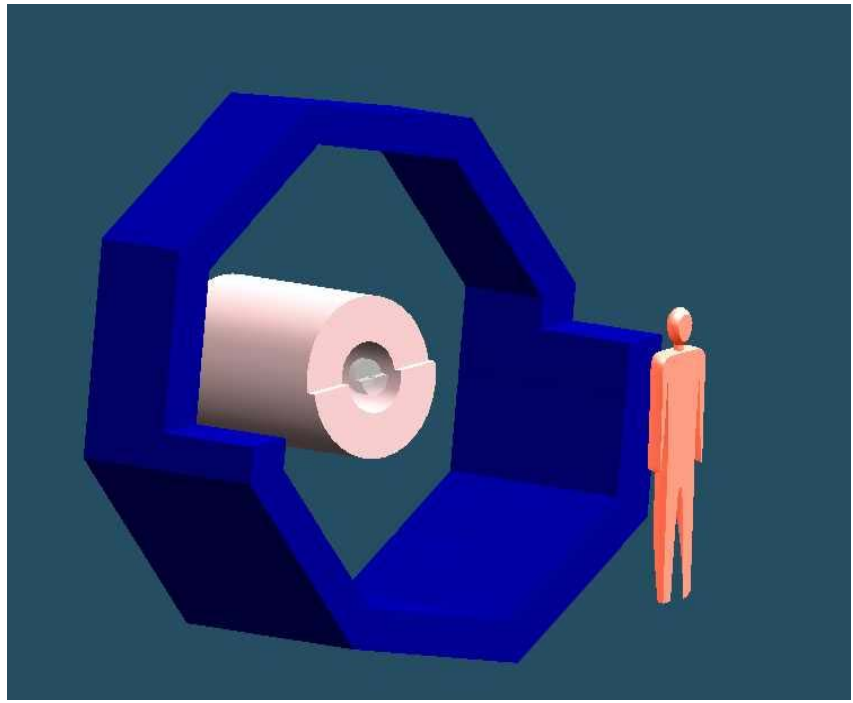
- *Accept* the notion that excellent energy flow calorimetry is required, and explore optimization of a Tungsten-Silicon EMCal and the implications for the detector architecture…

Architecture arguments

- Silicon is expensive, so limit area by limiting radius
- Get back BR^2 by pushing B (~5T)
- Maintain tracking resolution by using silicon strips
- Buy safety margin for VXD with the 5T B-field.
- Keep track finding by using 5 VXD space points to determine track – tracker measures sagitta.

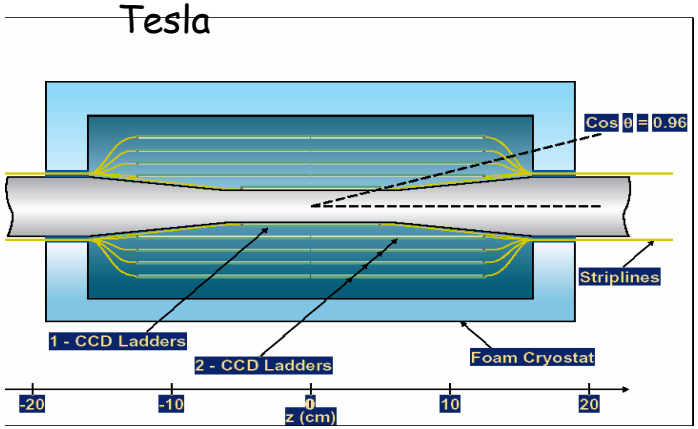
SiD Configuration

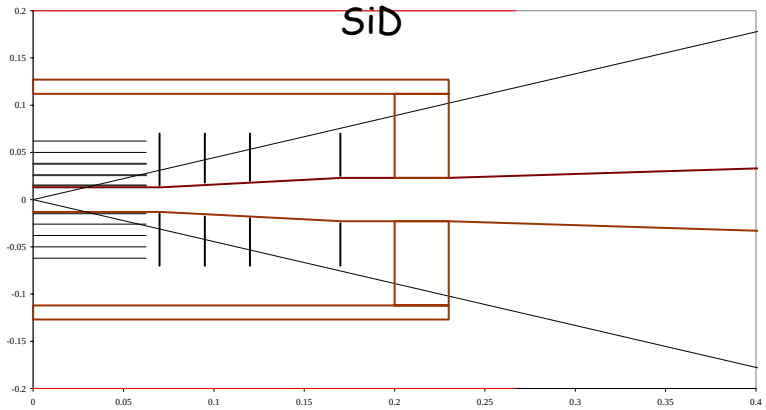




Scale of EMCal
& Vertex Detector

Vertex Detectors





Extend 5 layer tracking over max Ω
→improve Ω Coverage, improve σ_{xy}, σ_{rz}
5 CCD layers .97 (vs. .90 TDR VXD)
4 CCD layers .98 (vs. .93 TDR VXD)
Minimize CCD area/cost
→ Shorten Barrel CCDs to 12.5 cm (vs. 25.0cm)
Thin the CCD barrel endplate
→ a single 300 μm Si disk for self supporting

- Design CCD's for
  - Optimal shape ~2 x 12 cm
  - Multiple (~18) ReadOut nodes for fast readout
  - Thin -≤ 100 μ
  - Improved radiation hardness
  - Low power
- Readout ASIC
  - No connectors, cables, output to F.O.
  - High reliability
  - Increased RO speed and lower power compared to SLD VXD3
  - Detailed (preliminary) spec coming along…

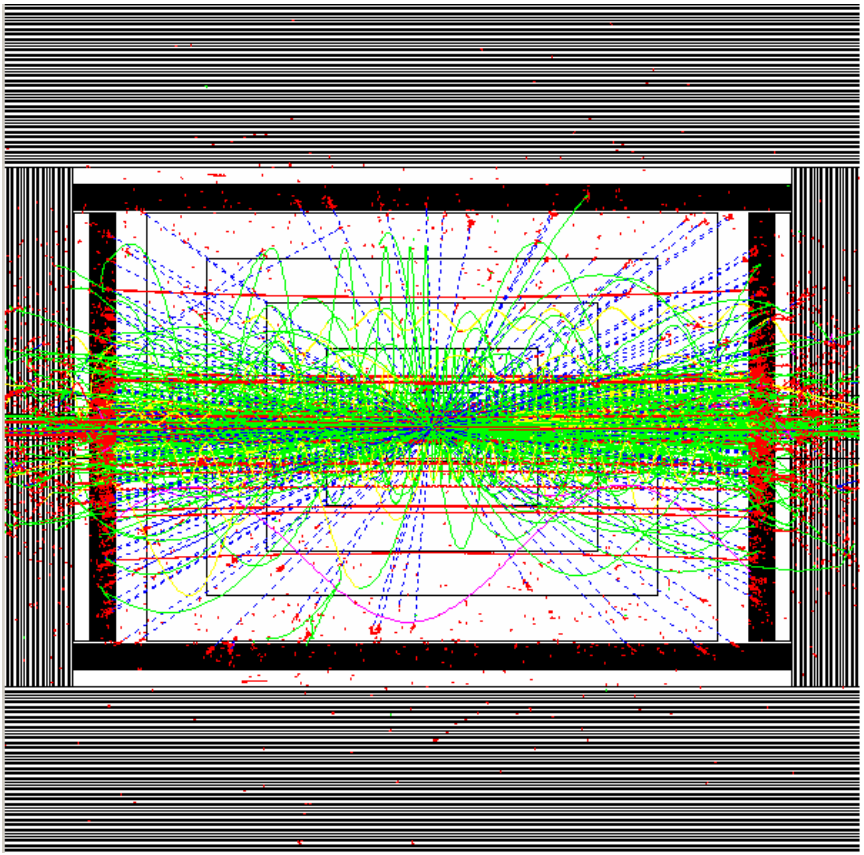
Vertex Detector Status

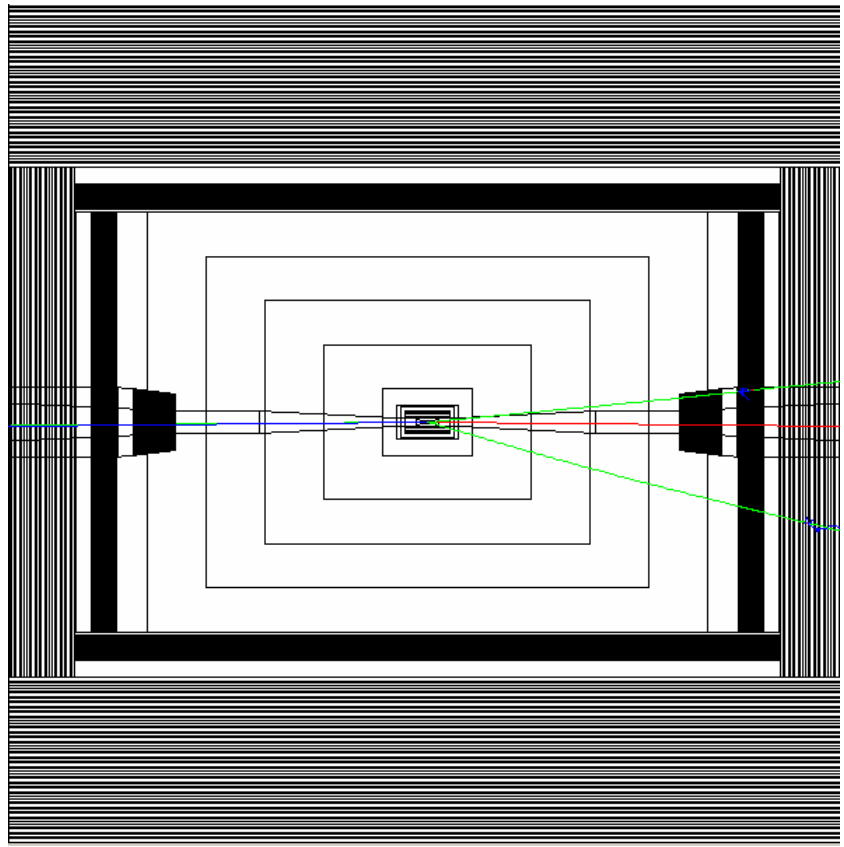
- Analysis of radiation damage to SLD VXD3 CCD's (N. Sinev/U. Oregon)
- Simulation studies concentrating on occupancy, radiation dose, and tracking performance. (T. Abe, N. Sinev)
- Full detector response simulated in LC, modelled after VXD3 performance (N. Sinev)
- Pattern recognition in LC environment (N. Sinev)
- No serious hardware development, but substantial interesting R&D work available on:
  - End plate CCD's (annular geometry)
  - Faster, harder devices (Oregon, Yale)
  - Readout ASICs (Oklahoma)

Silicon Tracker

- SLC/SLD Prejudice: Silicon is robust against machine mishaps; wires & gas are not.
- Silicon should be relatively easy to commission – no td relations, easily modeled Lorentz angle, stable geometry and constants.
- SiD as a *system* should have superb track finding:
  - 5 layers of highly pixellated CCD's
  - 5 layers of Si strips, outer layer measures 2 coordinates
  - EMCal provides extra tracking for Vee finding - ~1mm resolution!
- Simulation Studies:
  - Pattern recognition (S. Wagner)
  - Occupancies (T. Maruyama)
  - γγ backgrounds (T. Barklow)
  - Geometry optimization (R. Partridge - Brown)
  - All studies so far are encouraging. (Note very forward rates are high, and required segmentation is not yet (even conceptually) designed.
- Hardware develpments (just starting)
  - ASIC for long ladder readout (B. Schumm – UCSC)
  - Structure design "conversations" w SiDet group (FNAL)

Illustration of bunch timing tag





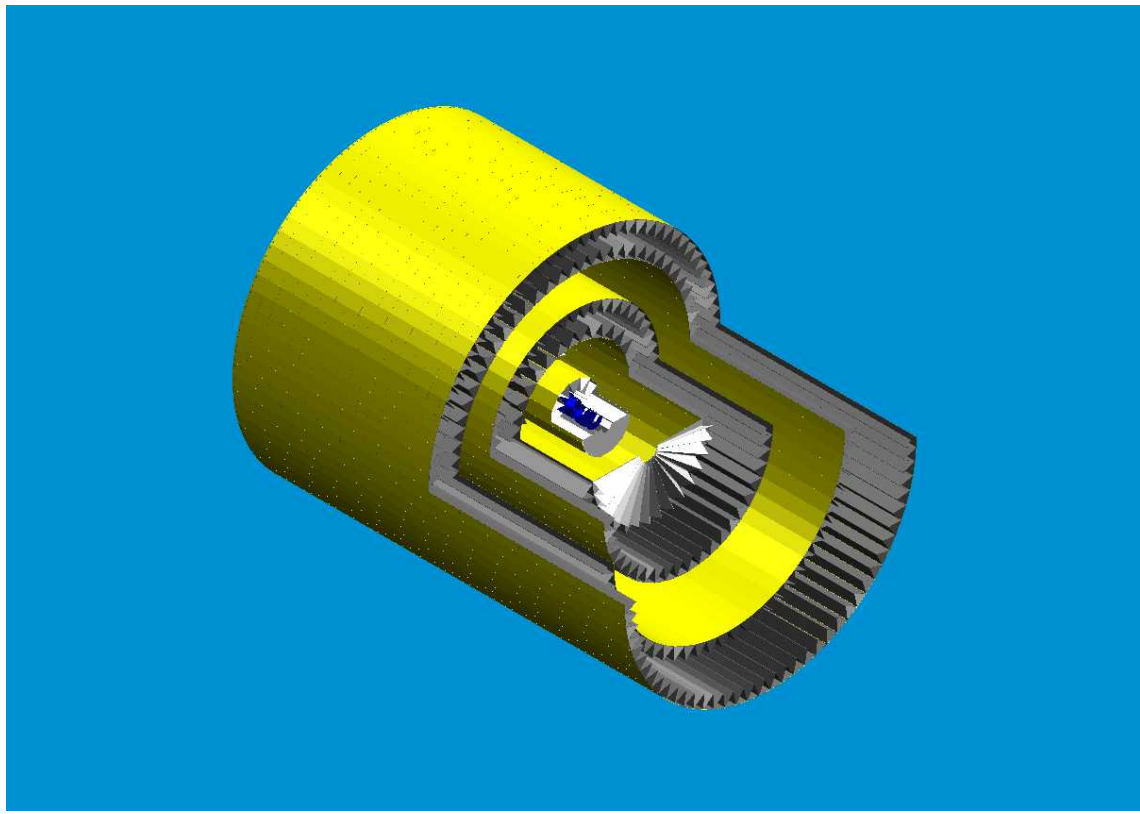
Yellow = muons Red = electrons Green = charged pions
Dashed Blue = photons with E > 100 MeV

full train (56 events)
454 GeV detected energy
100 detected charged tracks

1 bunch crossing

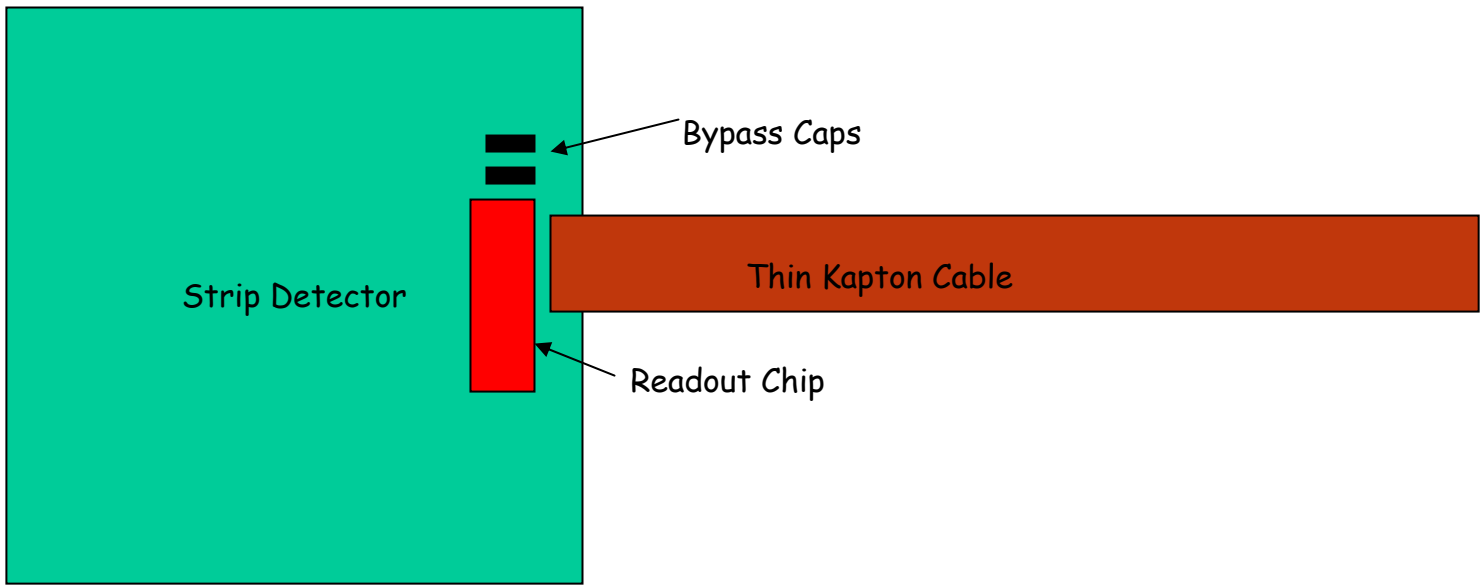
First attempt - Make Structure of Long Ladders

- Readout half ladders from ends.
- Wire bond 10 cm square detectors in daisy chain as in GLAST.
- Minimal electronics and power pulsing make gas cooling easy. No liquids, leaks or associated mass.
- Problems:
  - Timing tag seems impossible.
  - Occupancies forward

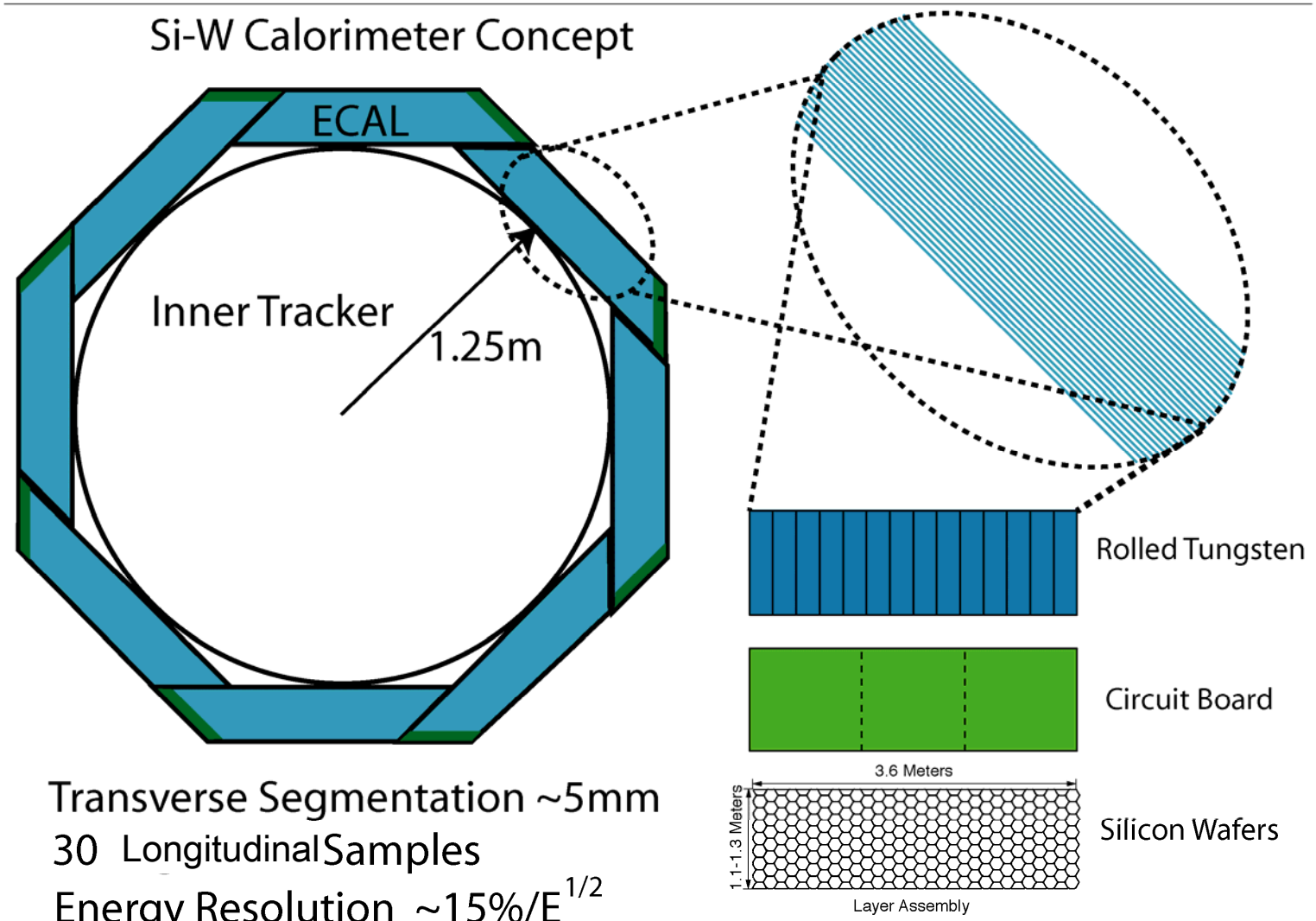


Evolve!

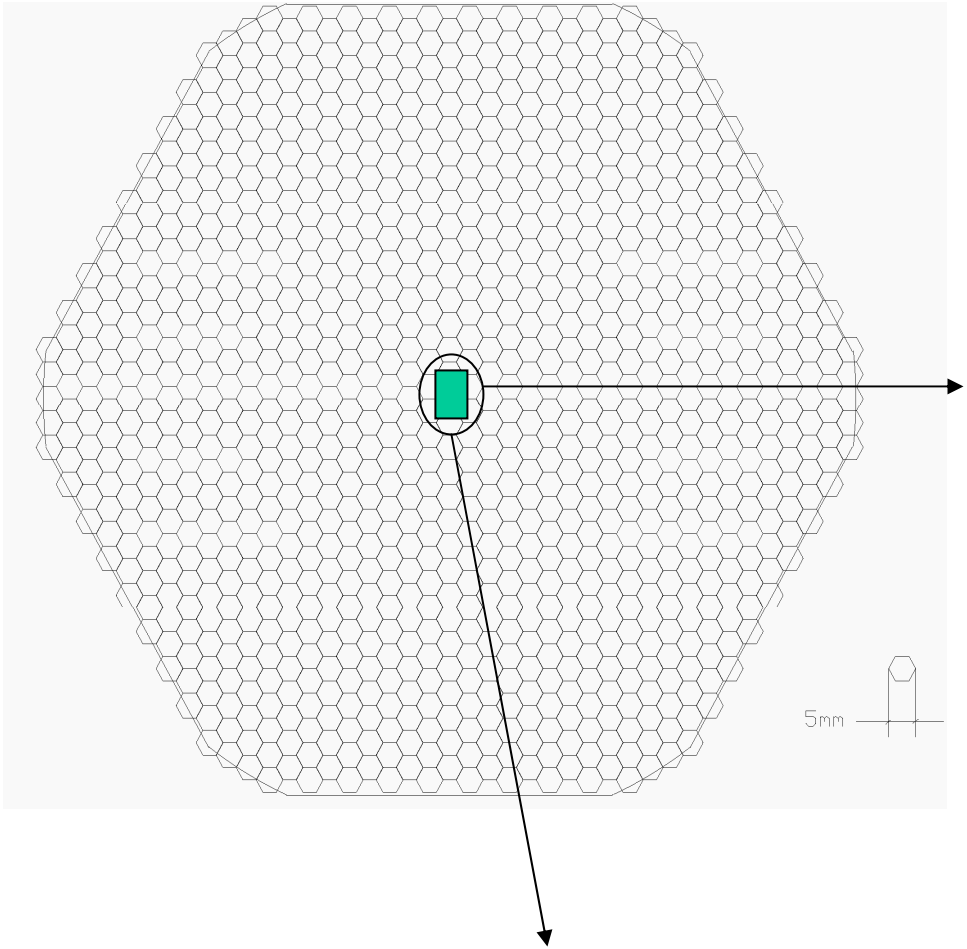
- Ditch (romantic) notion of long ladders and read out each detector.
- Detector has signals routed to rectangular grid for bump bonding to detector, analogous to design for Si-W Calorimeter.
- Bunch separation timing capability, better segmentation and occupancy, better S/N.
- Replace individual ladders with composite, monolithic cylinder with detectors mounted to surface.

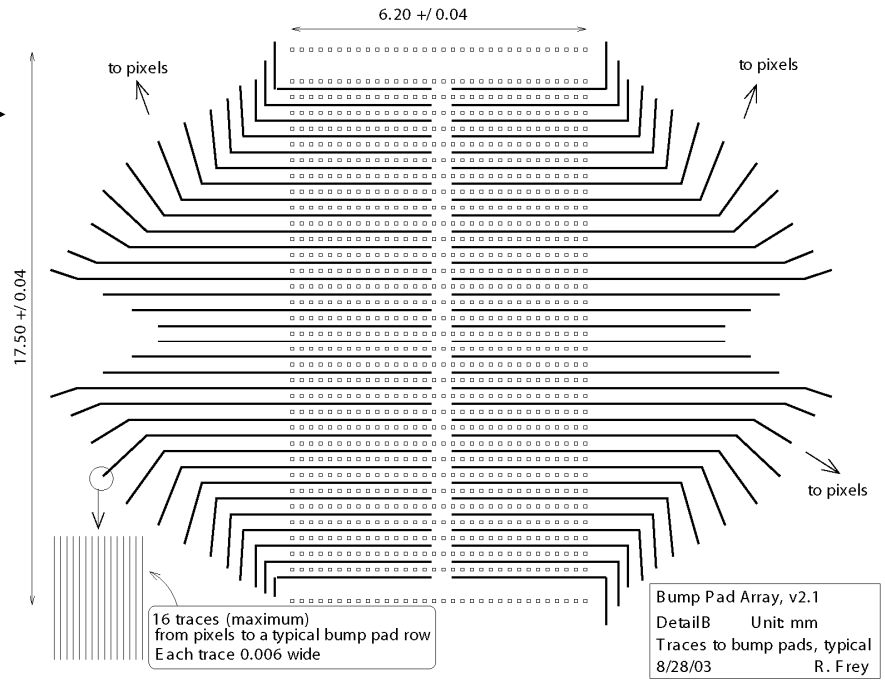


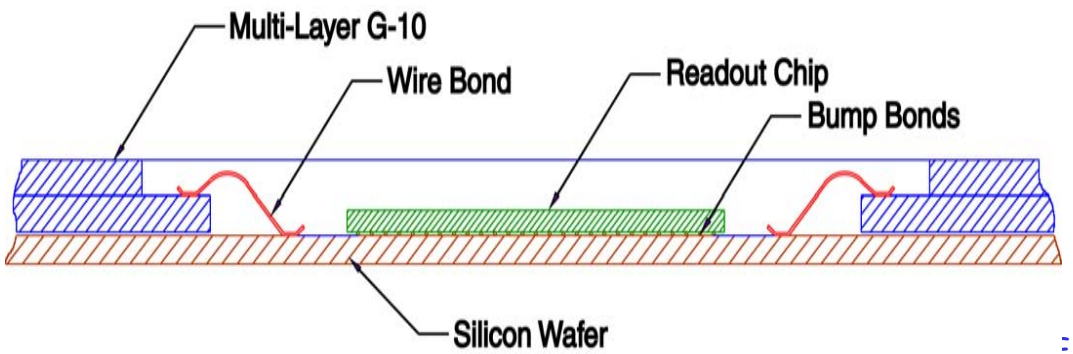
SiD EMCal Concept



Wafer and readout chip





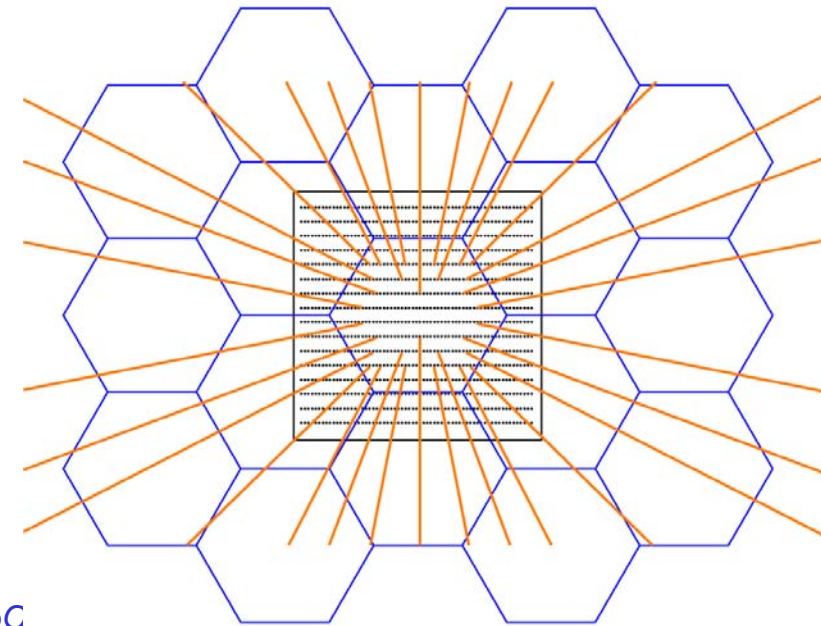


SiD Si/W Features

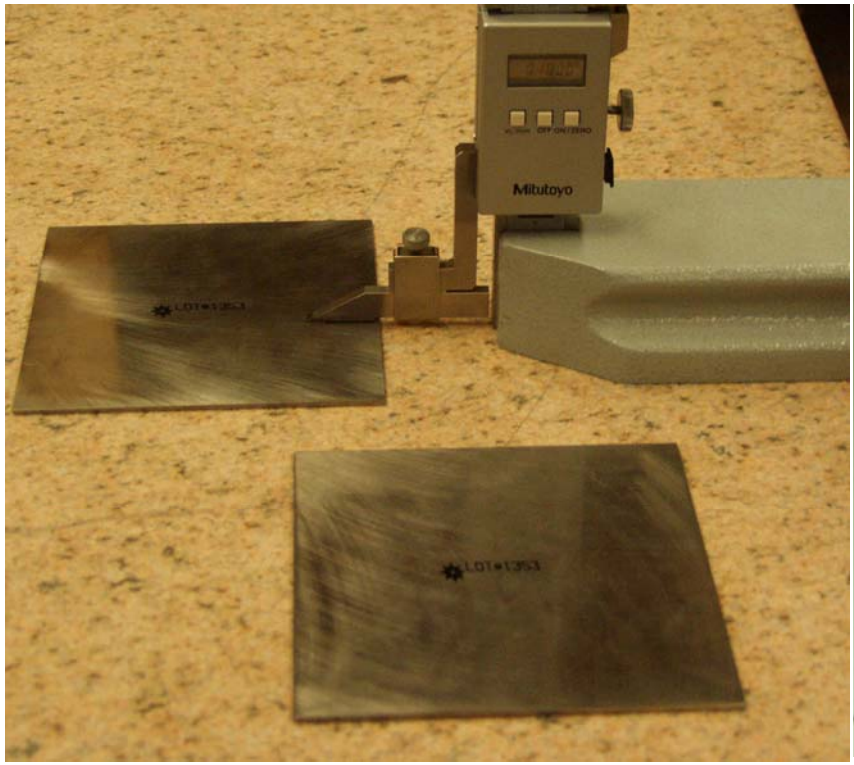
- "Channel count" reduced by factor of 10^3
- Compact – thin gap ~ 1mm
  - Moliere radius 9mm → 14 mm
- Cost nearly independent of transverse segmentation
- Power cycling – only passive cooling required
- Dynamic range OK
- BunchTiming in design
  - Low capacitance
  - Good S/N
  - Correct for charge slewing/outliers
  - 5 ns σ per measurement

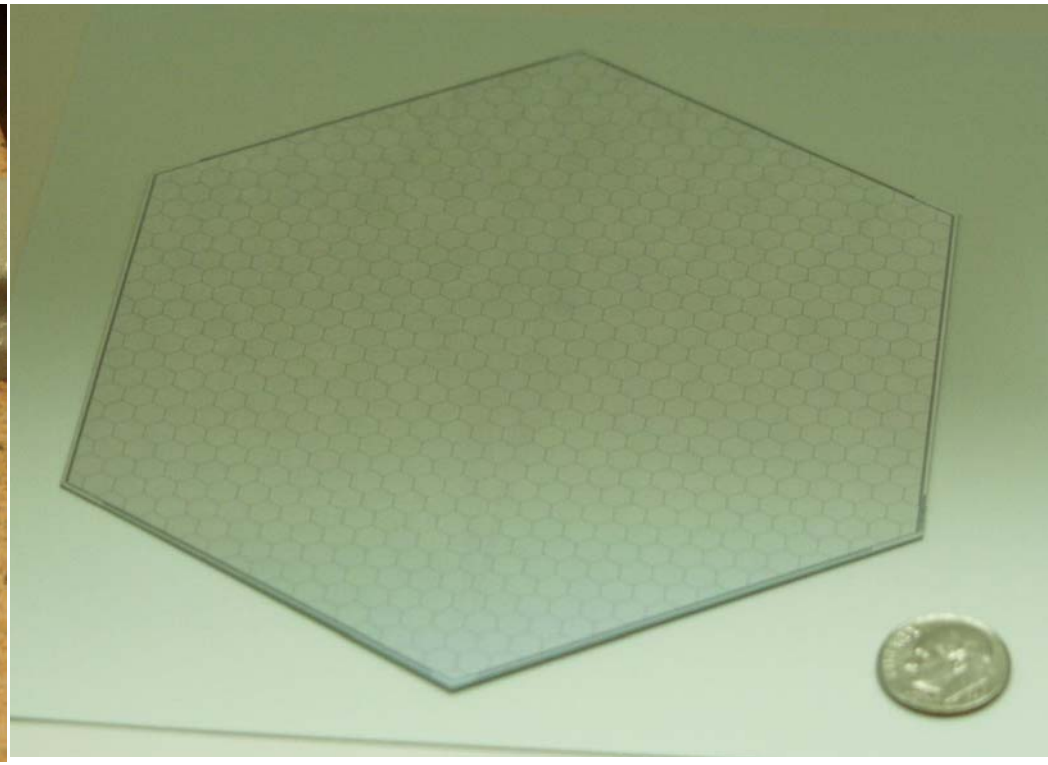
Current configuration:

- 5 mm pixels
- 30 layers:
  - 20 x 5/7 X0 +
  - 10 x 10/7 X0



Components in hand





Tungsten

- Rolled 2.5mm
  - 1mm still OK
- Very good quality
  - < 30 μm variations
- 92.5% W alloy
- Pieces up to 1m long possible

Silicon

- Hamamatsu detectors
- Should have first lab measurements soon

EMCal Status

- Primarily collaboration with U Oregon, BNL.
  - SLAC is designing very aggressive readout chip. (D. Freytag, O. Milgrome, G. Haller, mb)
  - U Oregon (R. Frey, D. Strom) working on actual detector.
  - Eventual goal is a test beam device ~30 X_0 thick, 1 wafer (hexagon ~15 cm across) transverse.
  - Need more effort on ASIC and mechanics.

ALPCG Working Group IP Beam Instrumentation

WG Leaders: M. Woods /E. Torrence/D. Cinabro
SLAC RD Physicists: M. Woods, T. Maruyama, T. Barklow, T. Abe, K. Moffeit

WG Scope ⟹ Beam Instrumentation required for LC Physics

Principle Topics

- Luminosity, luminosity spectrum (dL/dE)
- Energy scale and width
- Polarization
- Forward calorimetry for electron id and 2-photon veto
- also, instrumentation for optimizing luminosity:
  - IP BPMs for fast feedback and feedforward
  - detectors for pairs, beamsstrahlung, radiative Bhabhas

IP Beam Instrumentation

1. Letter-of-Intent, SLAC-LOI-2003.2, **Beam Instrumentation Tests for the Linear Collider using the SLAC A-Line and End Station A,** was submitted to SLAC and EPAC in November 2003. The response was encouraging. Expect to submit first test beam requests to the lab by mid-June. The LOI was submitted by 27 physicists from 10 institutions, including the UK.
3. Engineering design and simulation studies for the beam instrumentation are underway. Detailed studies to estimate the impact on physics analyses (ex. statistical and systematic errors for Higgs, top, SUSY analyses) given the expected beam parameters and performance of the beam instrumentation. This includes evaluating the impact of the warm-cold technology choice on the LC physics and LC detector design.
4. Evaluating the impact of the warm-cold technology choice includes:
   - bunch timing
   - energy spread
   - crossing angle

Timing Analysis!

- 2015 Begin Operation ???
- 6 years construction - 2009
- 3 years serious R&D - 2006
- 2 years – collaboration formation and conceptual design - 2004 [~now??]

Plans

- SLAC has a modest effort going in simulation and simulation tools, and an extremely modest effort in conceptual design and hardware.
- Goal is a CDR (a document outlining a design and explicitly showing the basis for the chosen parameters) in ~two years, based on the work of an SiD Design Study.
  - Imminent technology choice is increasing interest in LC.
  - H. Weerts (FNAL) & J. Jaros (SLAC) are organizing an international design study effort.
- The Design Study should help clarify detector R&D requirements.
- It is hoped that efforts at SLAC, FNAL, and LBNL will attract more university interest and DOE support.