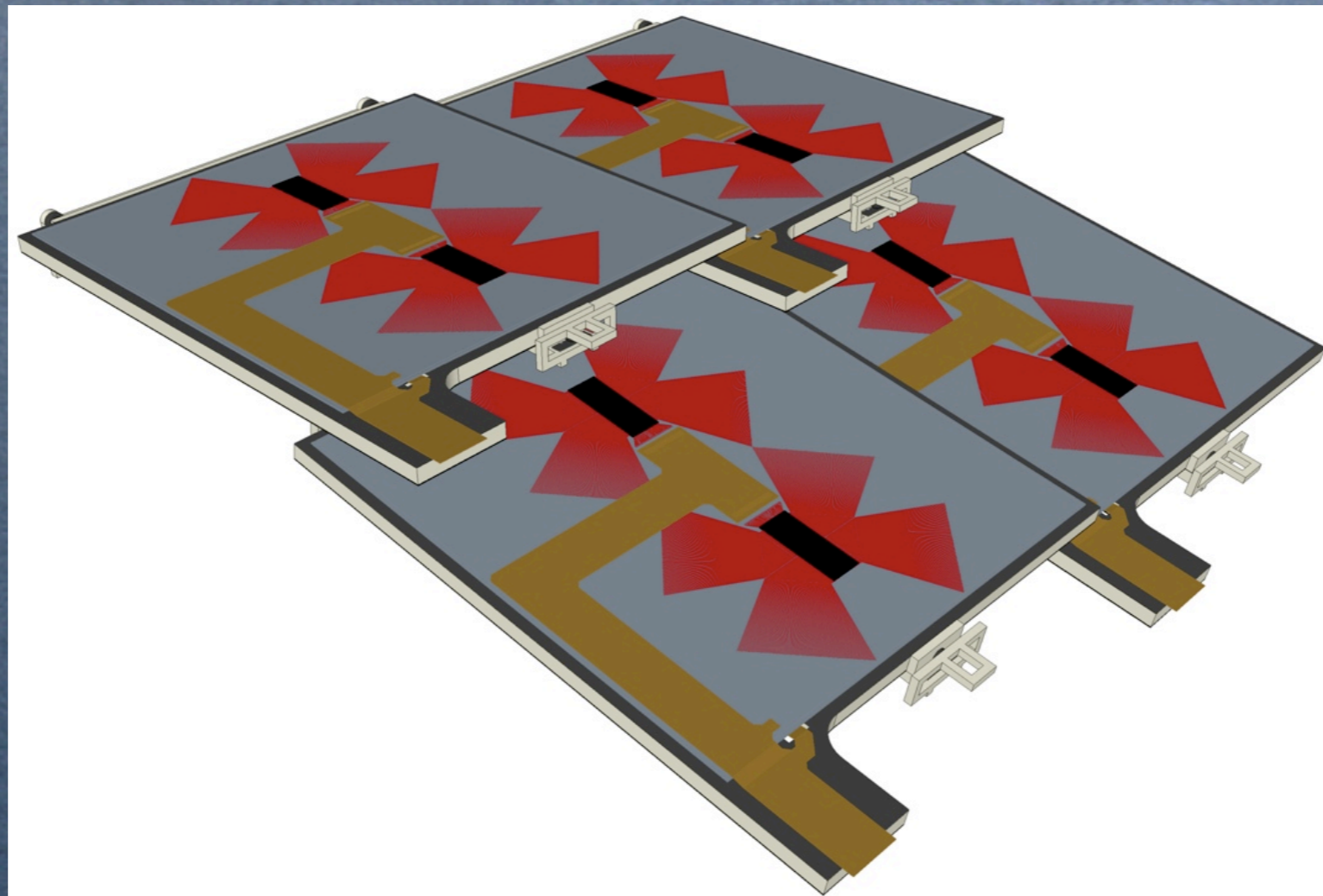


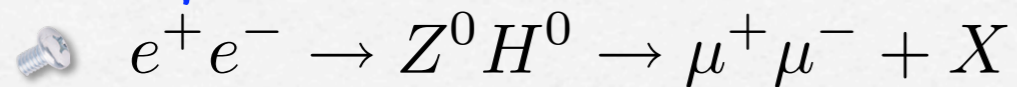
ILC Tracker R&D at SLAC



Tim Nelson

ILC Tracking Requirements

Superior P_T resolution:



Given $\sqrt{s}, M_Z, M_{\mu\mu} \implies M_H$



Fast readout:

- Long readout times add background to signal events
- Signal collection/readout time $\ll 100\text{ns}$

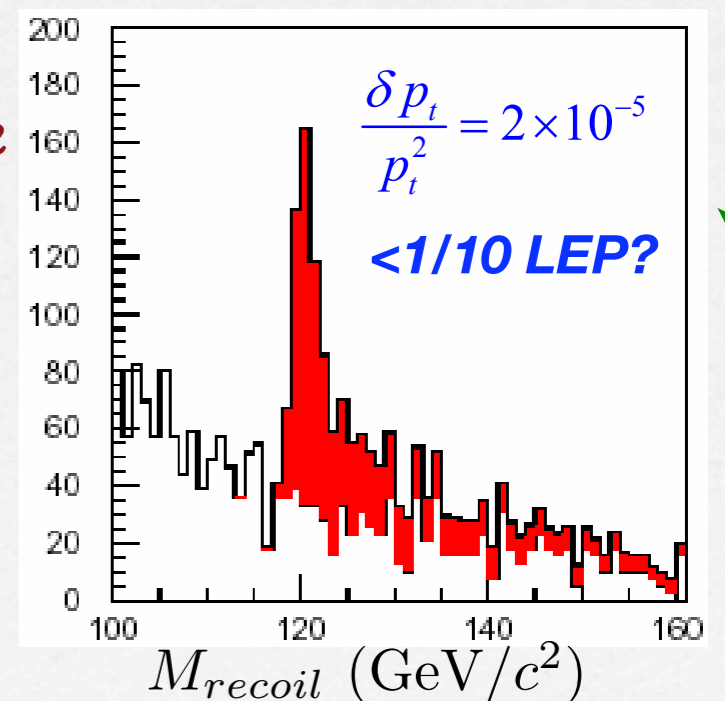
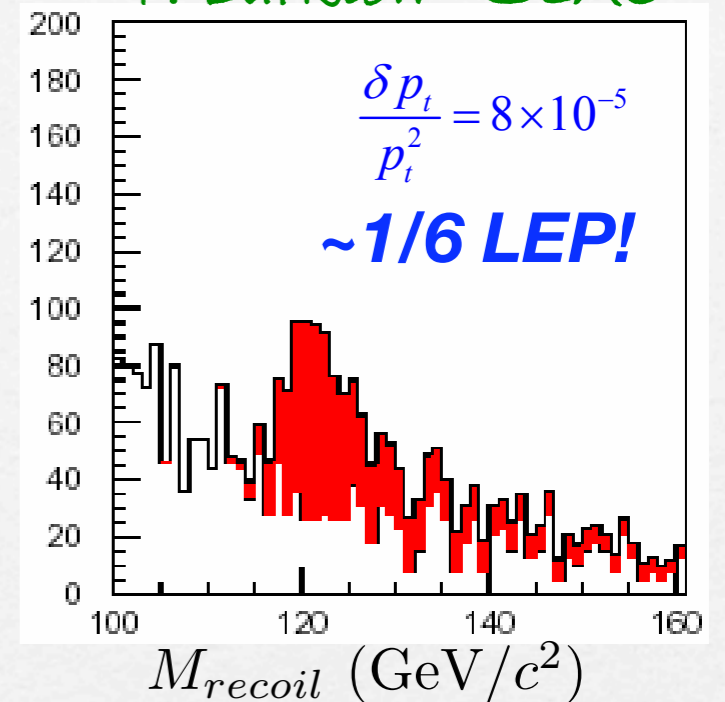
Low mass:

- Production of secondaries threatens calorimeter performance
- goal: average $< 1\% x_0$ / layer

Mass producible / low cost:

- Roughly same scale as LHC trackers
- Production of components must be simple

T. Barklow - SLAC



Possible Solutions

Superior P_T resolution:

- 🔩 Large radial span \Rightarrow SiW ECAL gets large, expensive
- 🔩 Large magnetic field \Rightarrow CMS-type solenoid of maximal field
- 🔩 Smallest single-hit resolution \Rightarrow Silicon, optimized for precision

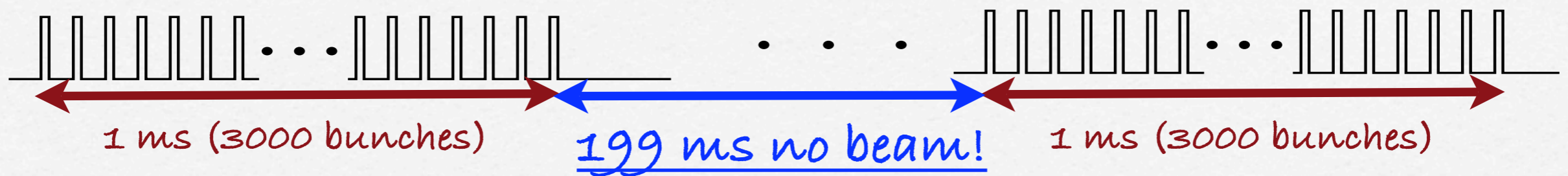
Fast Readout:

- 🔩 Solid state sensors \Rightarrow Silicon with beam-crossing time stamp

Low mass vs. Mass producible:

- 🔩 LHC did mass-producible silicon but NOT low-mass
- 🔩 BaBar did low-mass silicon but NOT mass-producible
 \Rightarrow Need a design that shatters this dilemma

Use ILC Machine Attributes



During collisions (0.5%):

- 🔩 Noisy digital functions of chip can be turned off
- 🔩 Need readout chip that stores analog signals during train
- 🔩 Simplifies isolation/filtering generally requiring a hybrid
⇒ Mass reduction AND assembly simplification

Between collisions (99.5%):

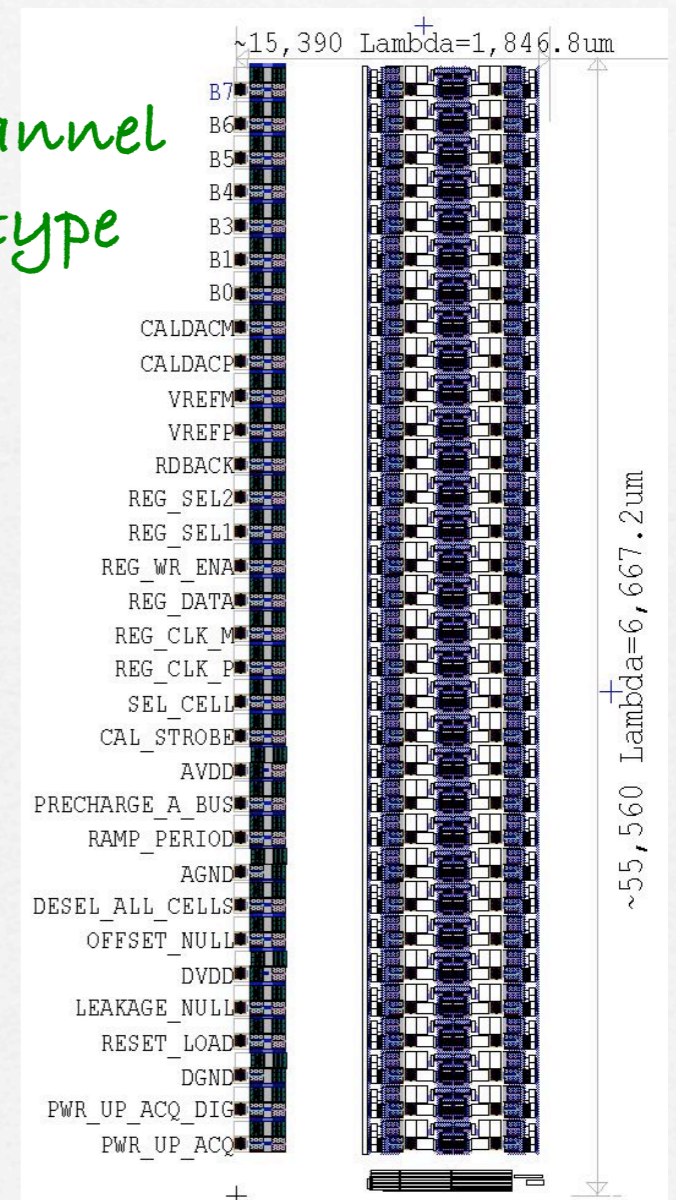
- 🔩 Power-consuming front-end can be powered down
- 🔩 Need readout chip that can be "power pulsed"
- 🔩 Eliminates need for active cooling
⇒ Mass reduction AND assembly simplification

KPiX Readout Chip

Already under development
at SLAC for SiD ECAL!

- 1024 Channels
- Power-pulsed, average power $\sim 20\text{mW}$
- 4 time-stamped analog buffers for readout between trains
- Designed for bump-bonding directly to silicon - no hybrid
- Dual-range logic is only extraneous component

64-channel
prototype



All the basic attributes we require

Optimizing Single-hit Resolution

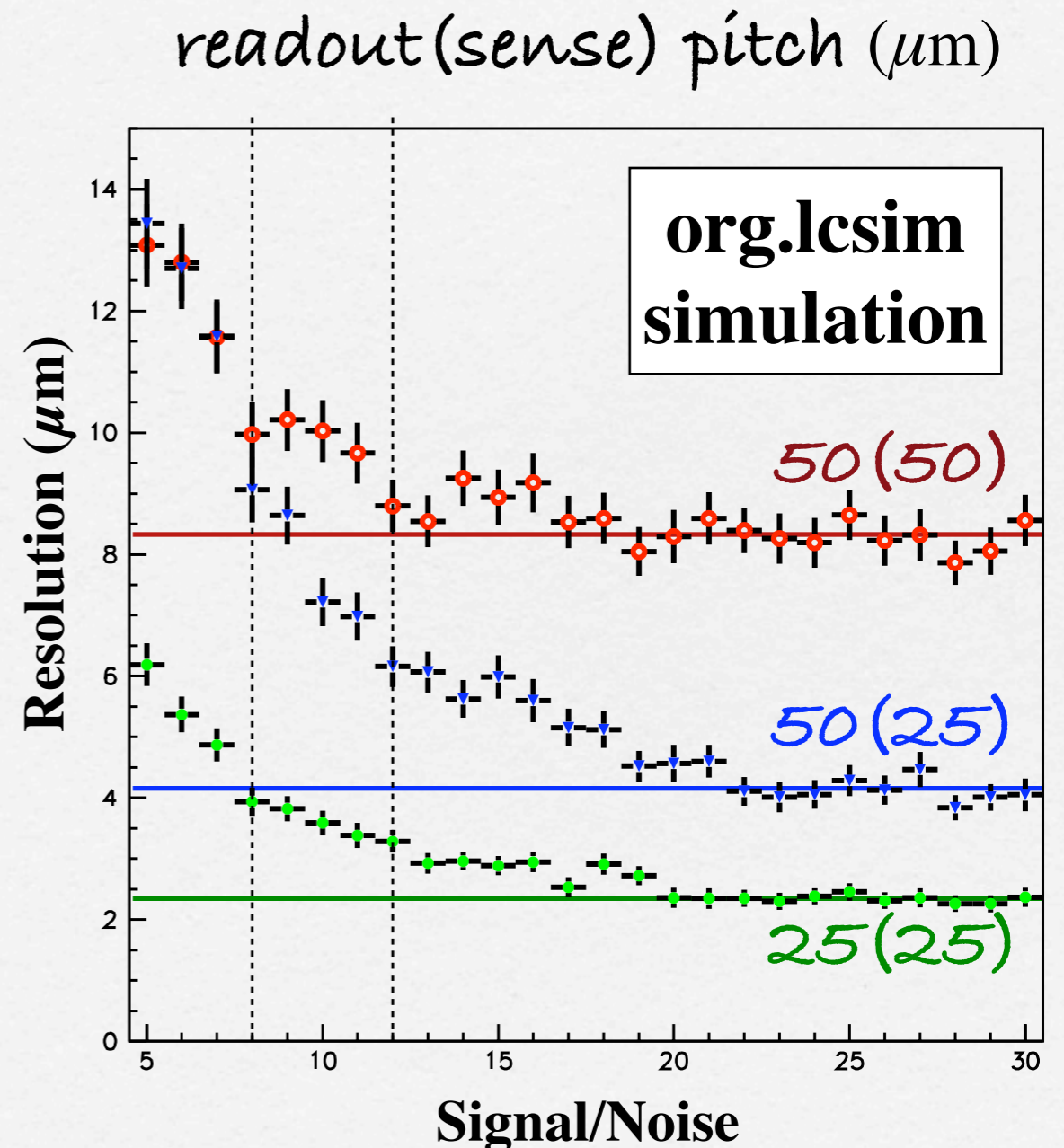
Reduce sense pitch ($> 25 \mu\text{m}$)

🔩 Huge channel count/density:
readout becomes difficult
⇒ Read out every-other channel

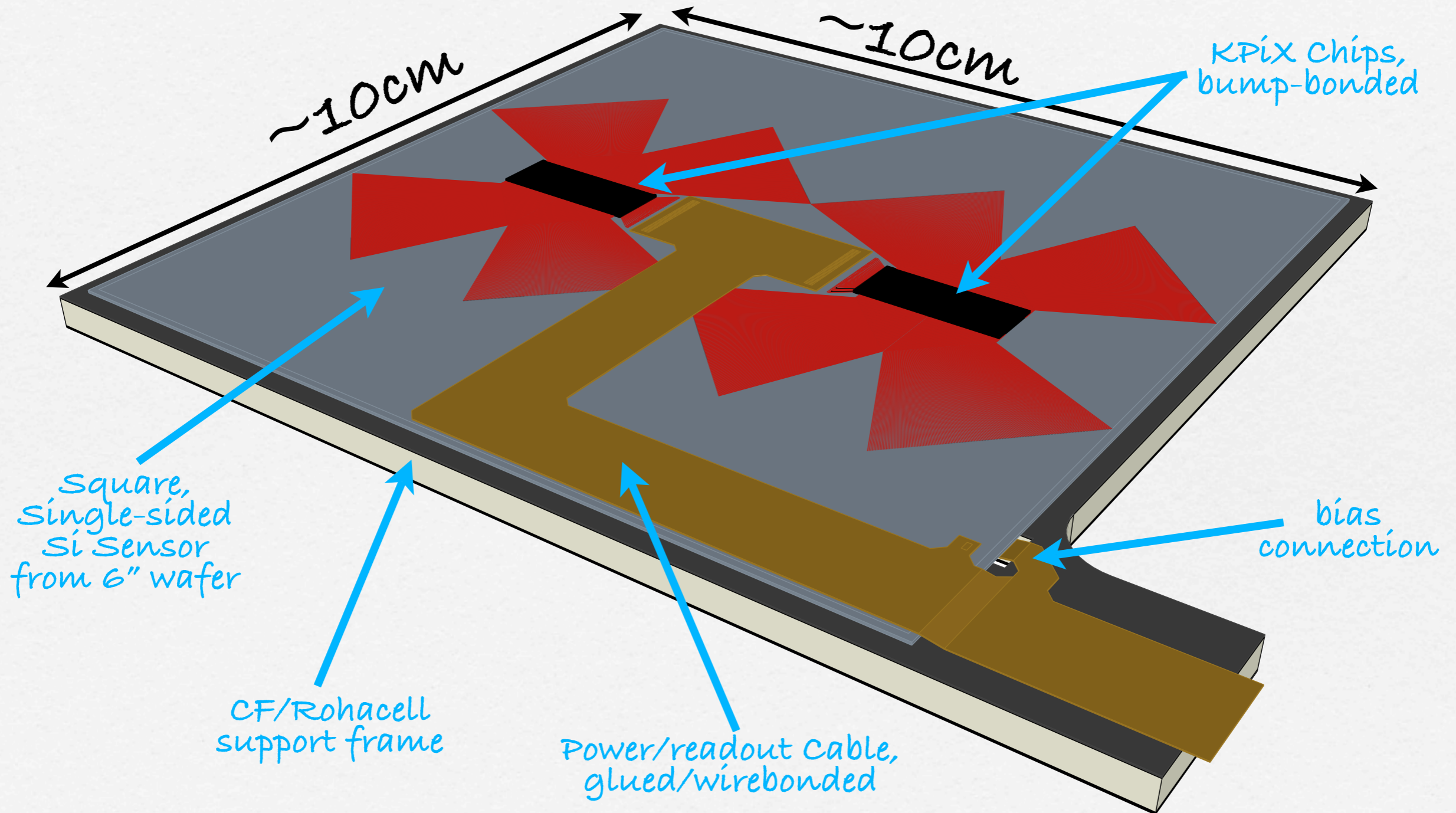
🔩 Delivers resolution that
approaches full 25 micron
readout for high S/N

🔩 Requires high S/N to deliver best
performance

⇒ Short strips for small
input capacitance on amplifier



Short Module Design

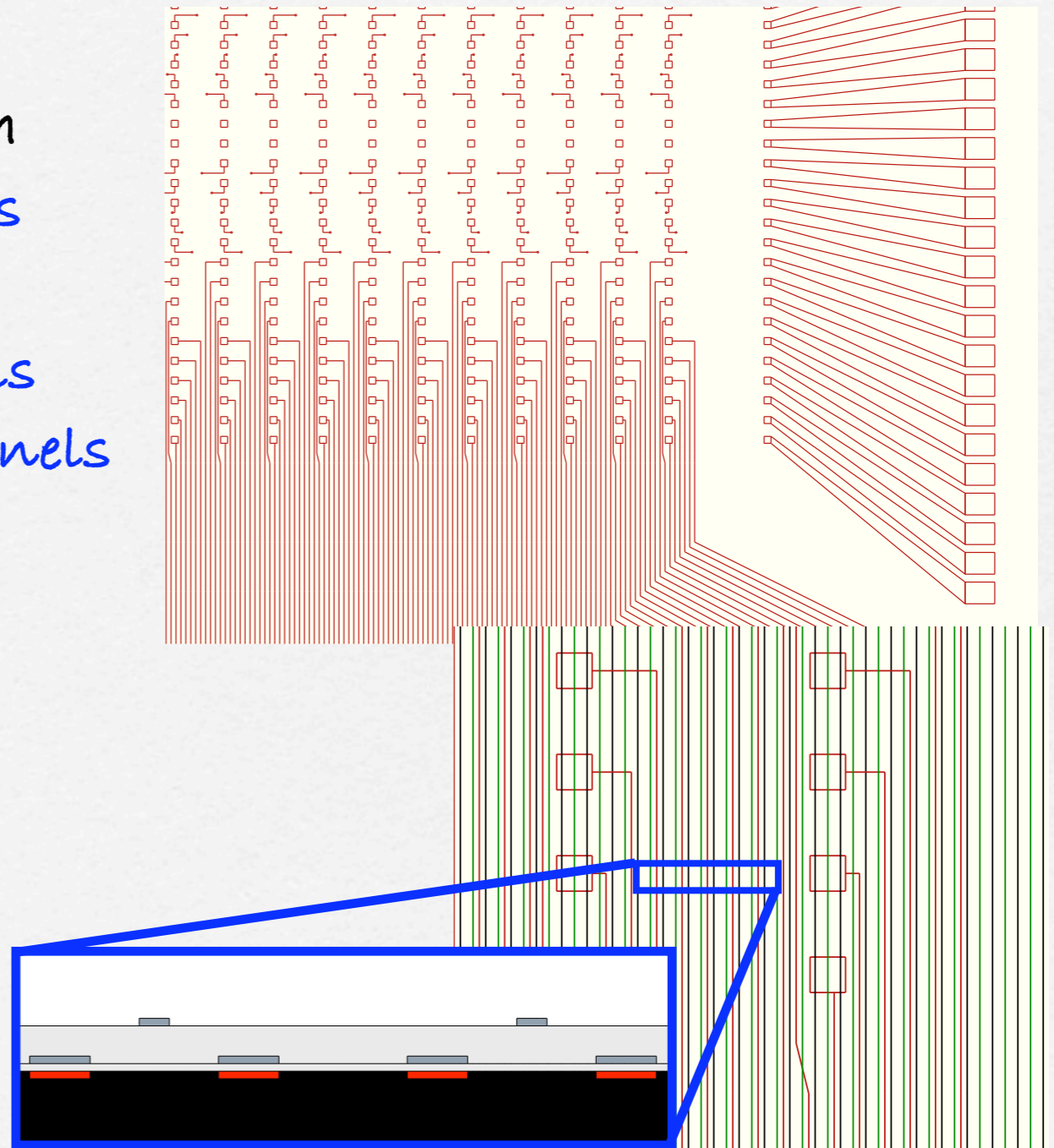


Sensor Design

- Single-sided p-in-n silicon
- 50 (25) micron readout (sense) pitch
- Double-metal carries digital signals and power between cable and KPIX
- Double-metal readout carries signals to KPIX bonding array:
1856 channels
 - Shortest trace: 15pf, 225 ohms
 - Longest trace: 21pf, 490 ohms

Should achieve $S/N > 25$

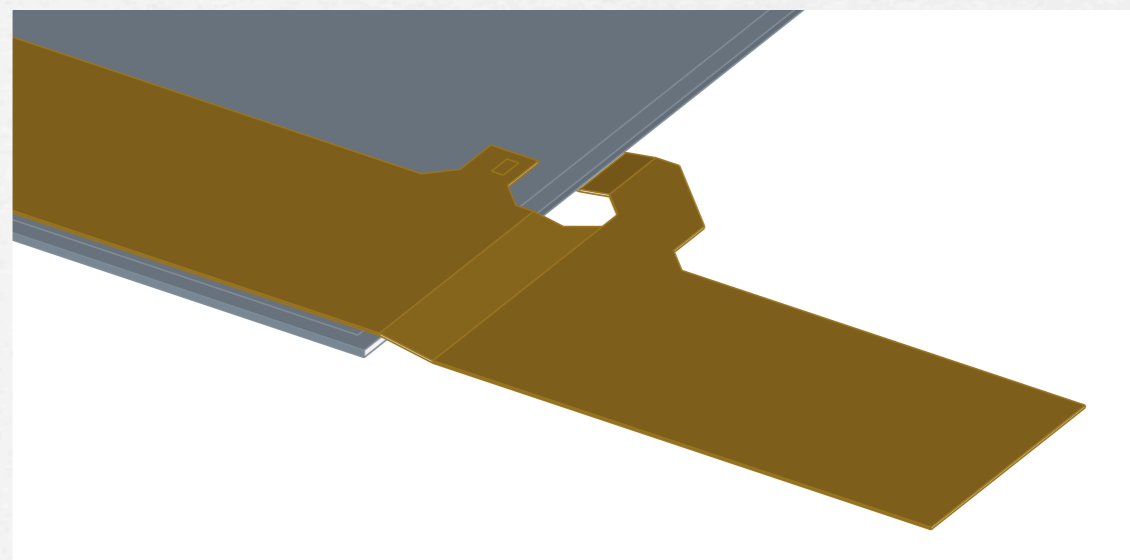
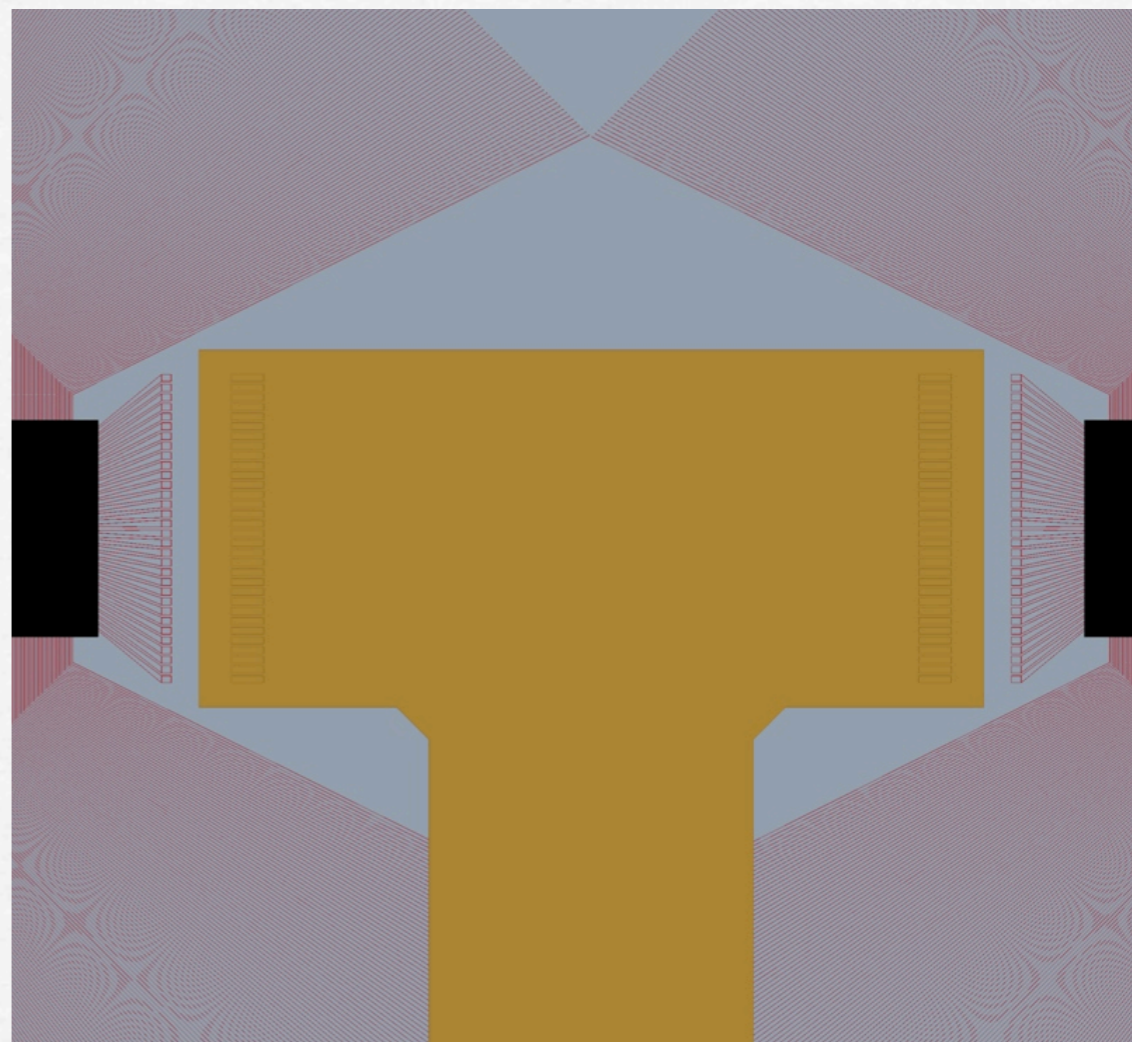
- ➔ Preparing detailed design and specs for HPK with FNAL
- ➔ Submit this fall (w/ ECAL)



Cable Design

- 🔩 pigtail glued & wirebonded to sensor
- 🔩 very simple extension cable to electronics at ends of barrel cylinders
- 🔩 will follow the lead of similar ECAL cable design underway now
- 🔩 *no group currently covering cable design*

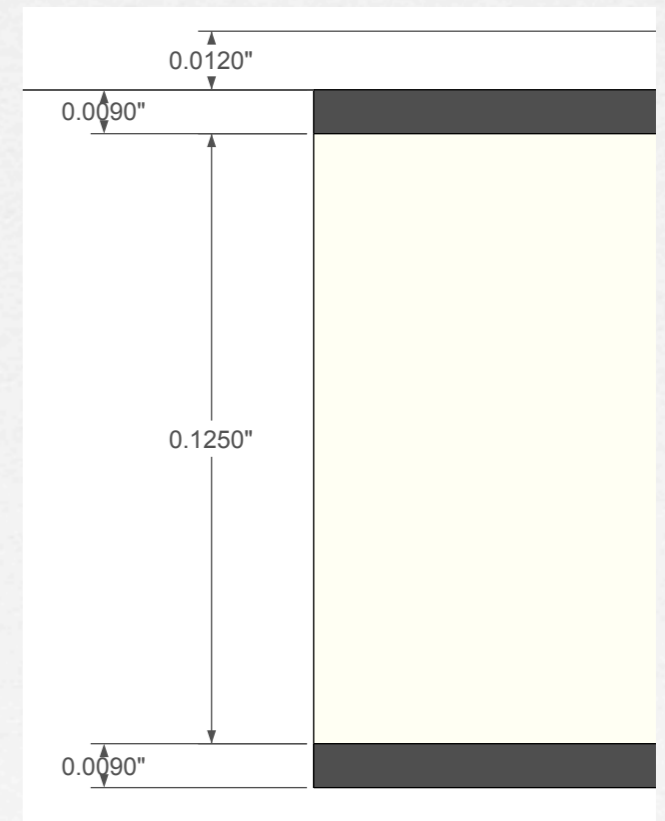
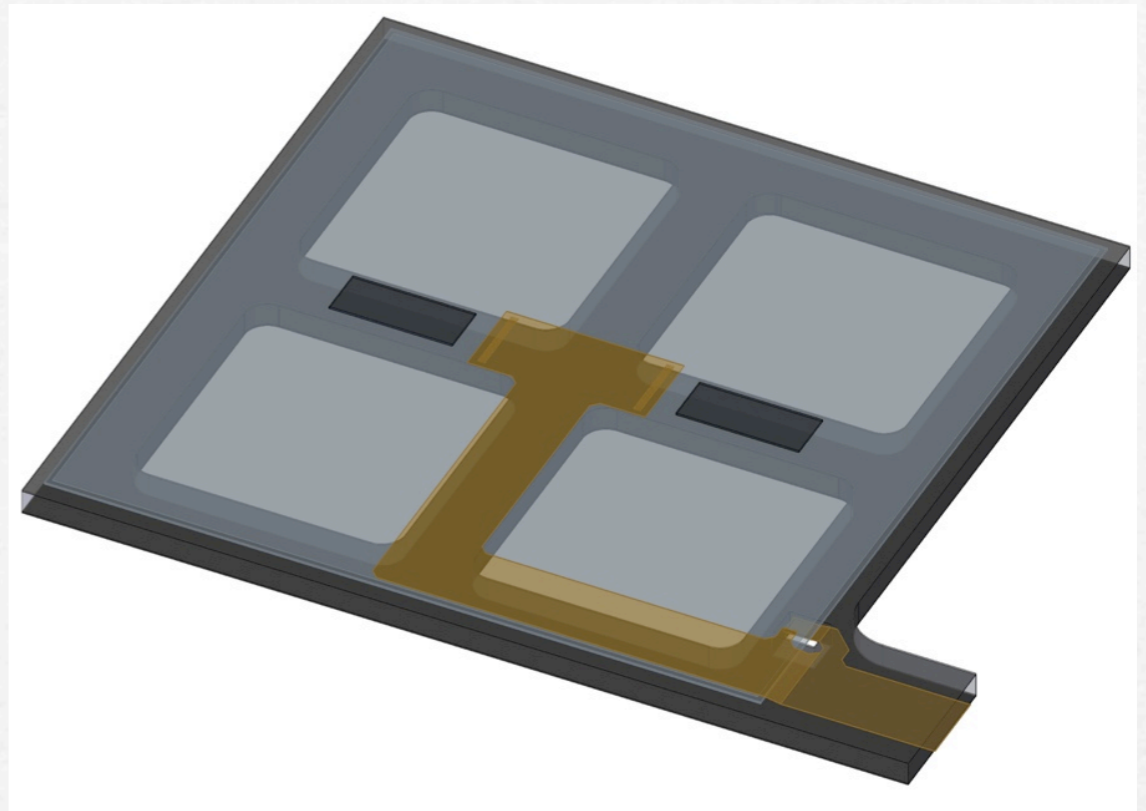
- ➡ Need to develop design for pigtail cable
- ➡ Need to develop design for extension cable



Module Support

Low-mass, mass producible

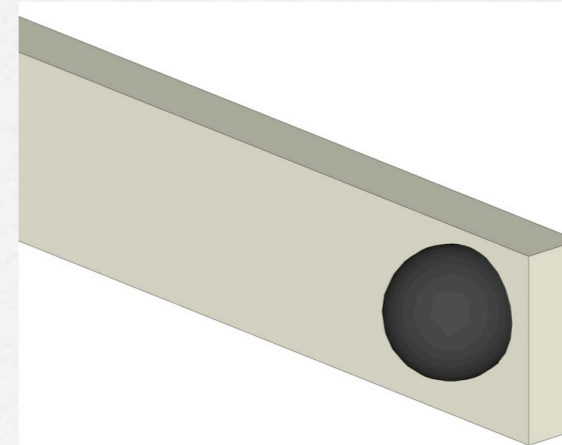
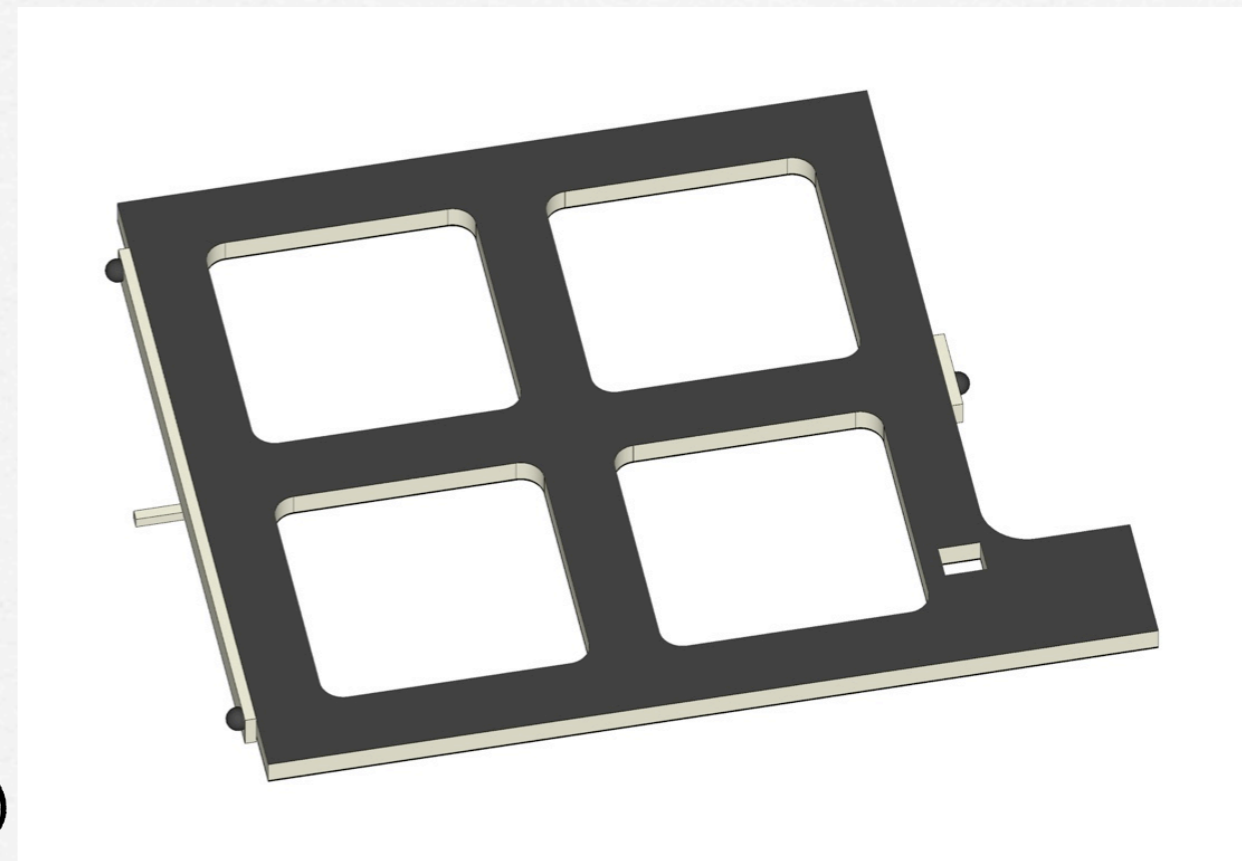
- Two, 60°-60°-60°, 0.009" thick, high-modulus CF sheets
 - 0.125" Rohacell foam sheet
 - 50% void, but CF directly under KPIX
 - Only enough mass to hold silicon flat: $\sim 0.15\% \times_0$
 - tab for handling, cable strain relief
- ➔ FEA to see if it is enough/too-much: FNAL / U Wash.
- ➔ Investigate cost of production by industry
- ➔ prepare tooling for prototypes



Module Mounting

High-precision, low-mass,
mass-producible mounts

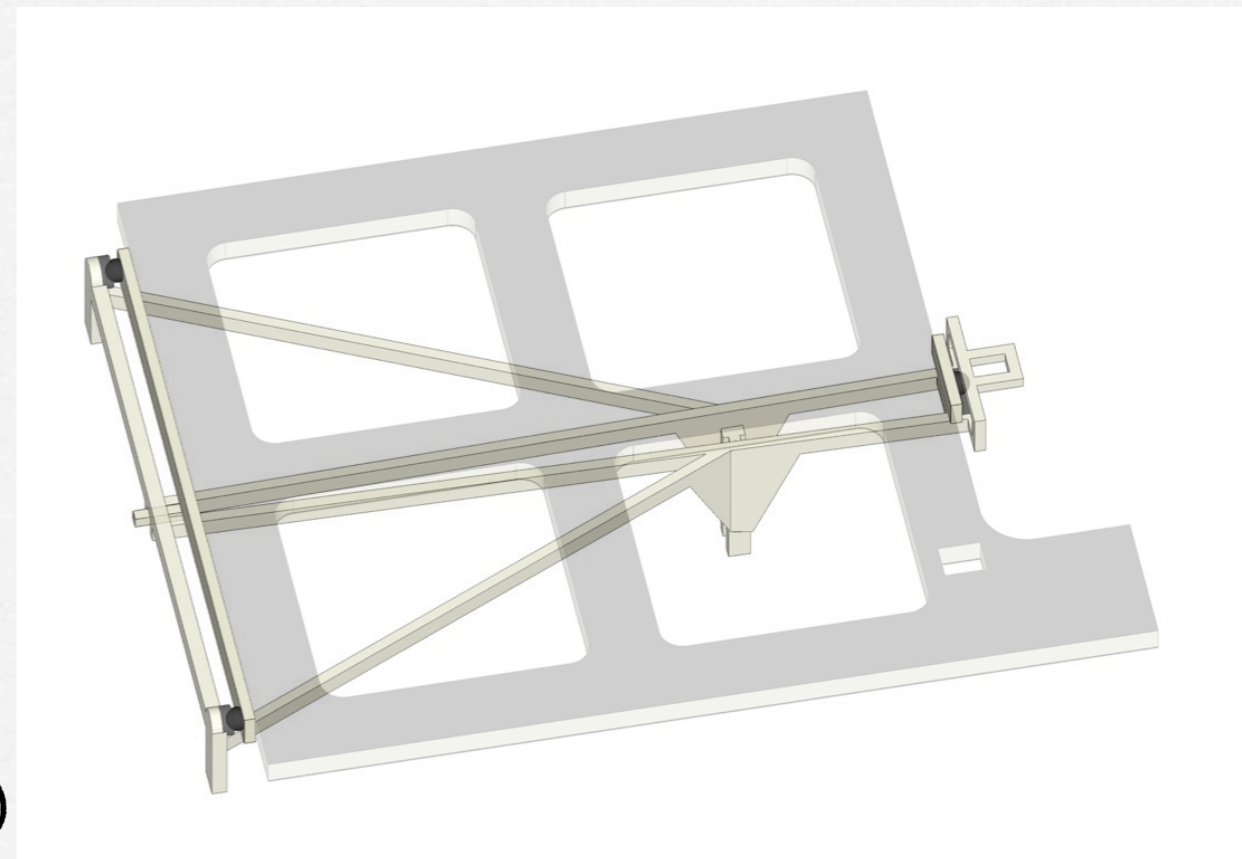
- CF-filled, PEEK or Torlon
(working with Victrex, Solvay)
 - high modulus
 - low CTE (near Si)
 - can be injection molded
- Insert-molded silicon-nitride
mating parts (input from Ceradyne)
 - long radiation length (\sim Si)
 - high-precision (< 1 micron)
 - very hard, low friction



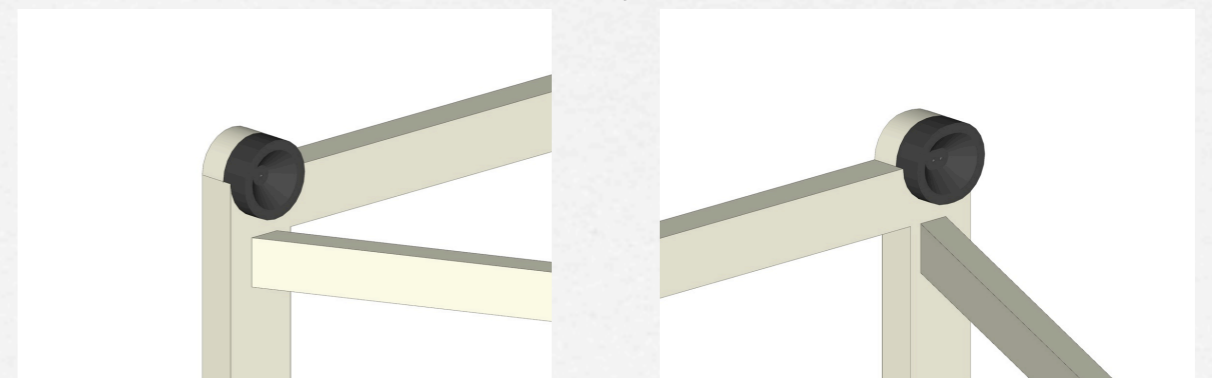
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mating parts (input from Ceradyne)
 - long radiation length (\sim Si)
 - high-precision (< 1 micron)
 - very hard, low friction
- FEA of mounting clip: FNAL/UW
- Mold design and quotes for plastic
and ceramic components



$\sim 0.1\% \times 0$



Overall Support

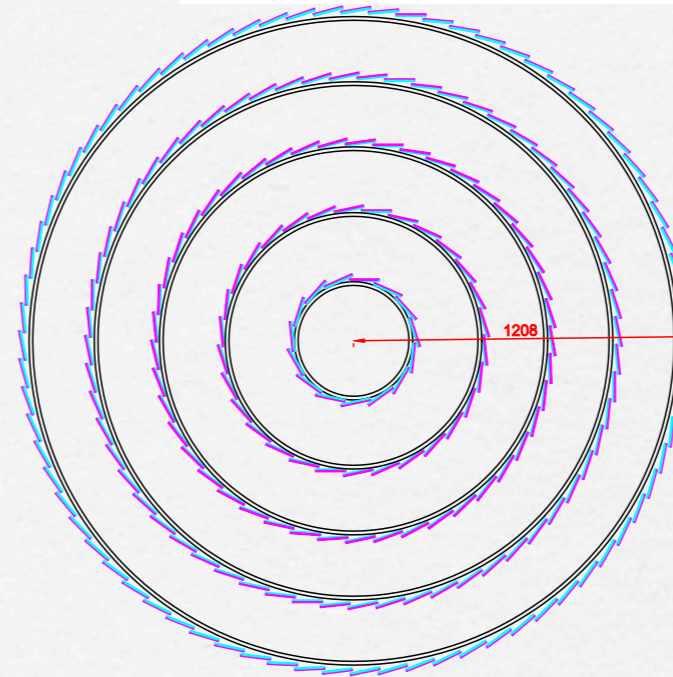
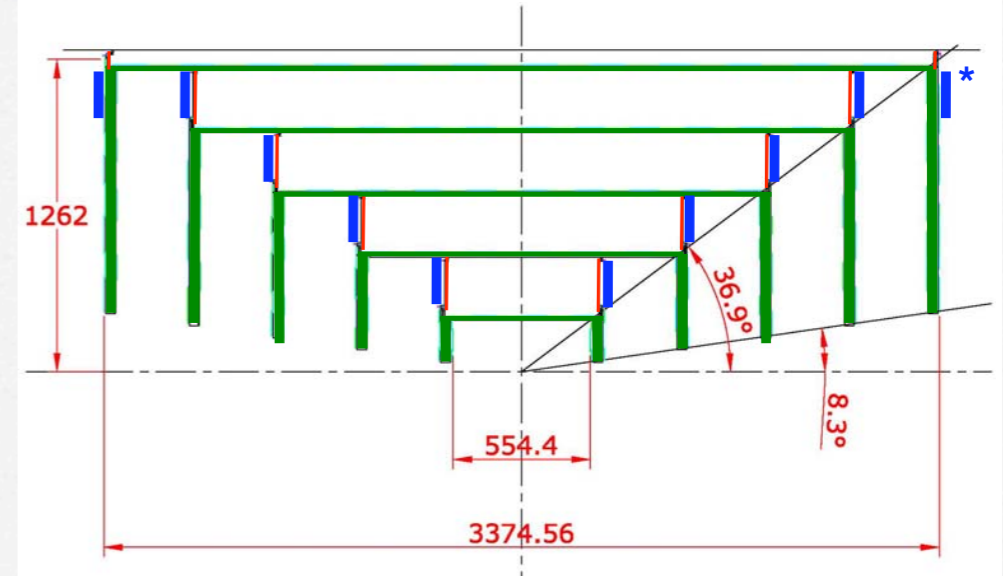
Short modules need many mount points:

➔ CF/Rohacell cylinders
(DO CFT and ATLAS SCT)

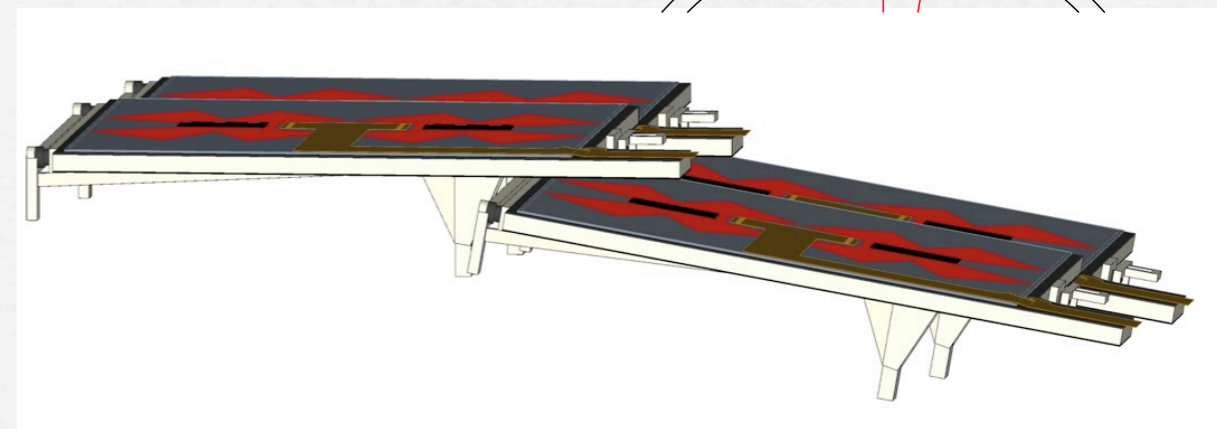
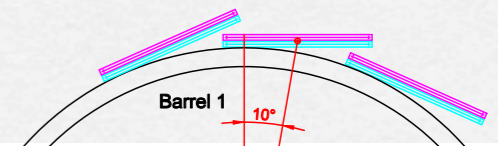
very low mass ($\sim 0.25\% X_0$)
maximally rigid single unit

FNAL engineering of cylinders,
tiling design encouraging

➔ Work closely with FNAL on module mounting
➔ Develop realistic power/readout distribution system



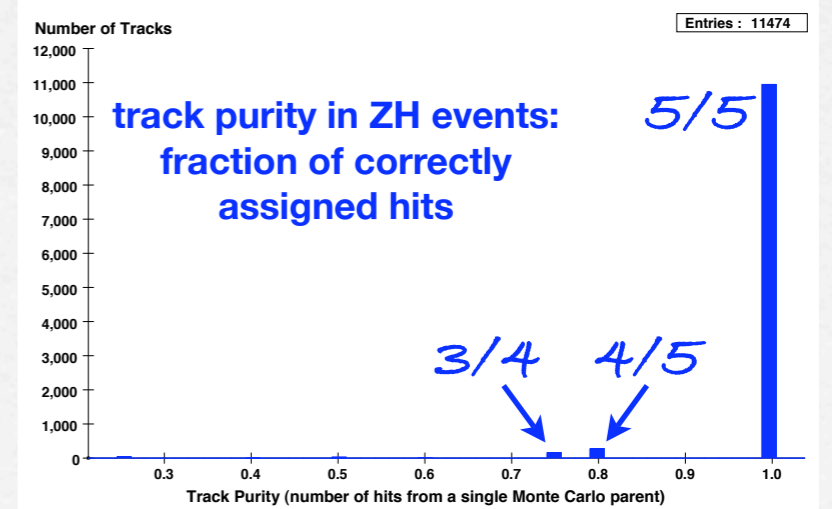
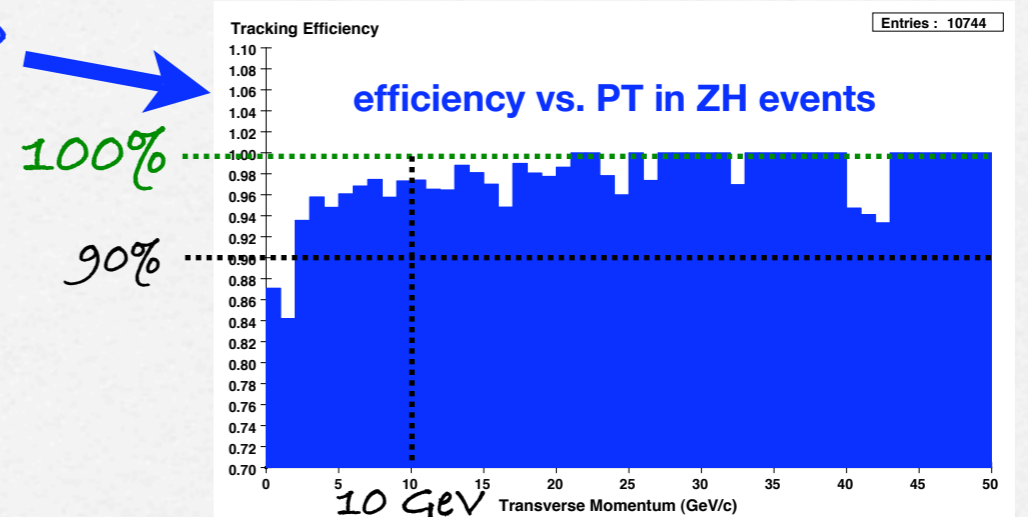
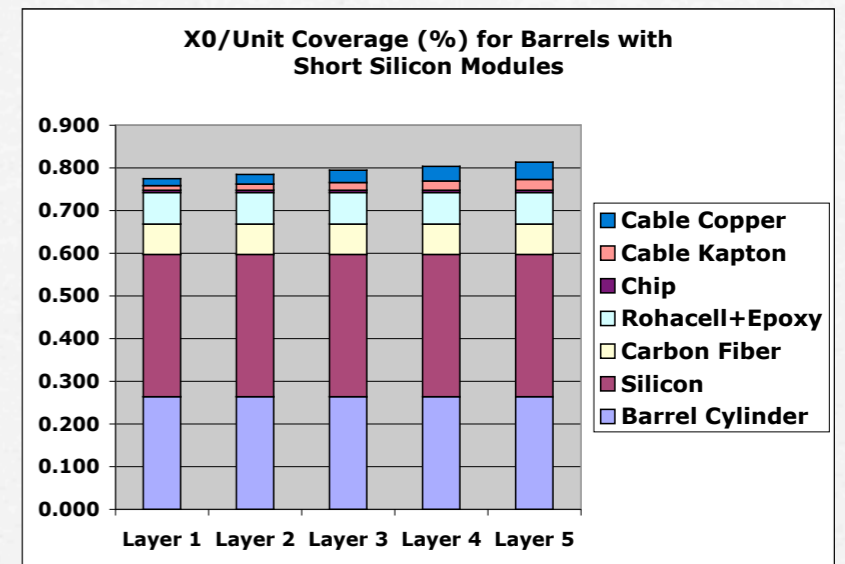
Sensors:
Cut dim's: 104.44 W x 84 L
Active dim's: 102.4 W x 81.96 L
Boxes:
Outer dim's: 107.44 W x 87 L x 4 H
Support cylinders:
OR: 213.5, 462.5, 700, 935, 1170
Number of phi: 15, 30, 45, 60, 75
Central tilt angle: 10 degrees
Sensor phi overlap (mm):
Barrel 1: 5.3
Barrel 2: 0.57
Barrel 3: 0.40
Barrel 4: 0.55
Barrel 5: 0.63
Cyan and magenta sensors and boxes are assumed to be at different Z's and to overlap in Z.
Within a given barrel, cyan sensors overlap in phi as do magnet sensors.



Tracking Studies

Model of tracker in simulation:

- Are 5 layers enough?
 - How much material is too much?
 - Does tracker need standalone capability?
(drives assembly precision)
 - Do we need double-sided layers?
(N.B. studies show short modules provide useful z-information!)
 - What do the endcap modules need to look like?
- A detailed simulation and complete reconstruction toolkit are required
a big job...more manpower needed



SiD Tracker R&D Roadmap

2006

- Obtain prototype silicon, begin probing and testing with KPIX
- Design prototype pigtail cables (needs new effort)
- Produce fully engineered module design incl. costing
- Produce fully engineered module mounting scheme incl. costing

2007

- Obtain prototype pigtails, testing/assembly/wirebonding with sensors
- Obtain/fabricate prototype module supports, mechanical testing
- Develop module assembly fixtures and assemble first prototype module
- Develop design for endcap modules (needs tracking studies)
- Develop power distribution system

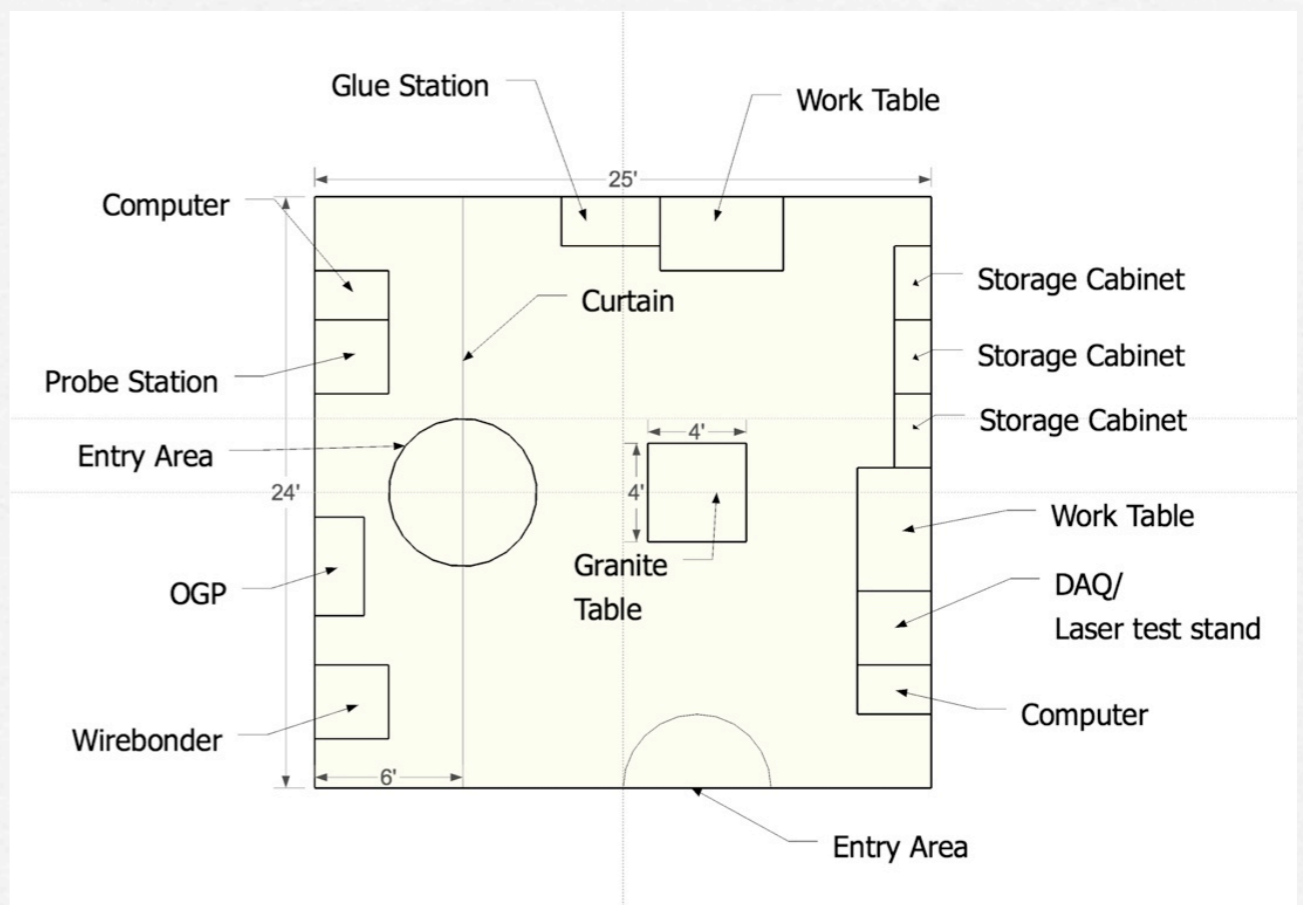
2008

- Assemble telescope of ~10 prototype modules for beam test
- Begin prototyping of endcap modules

Laboratory Facilities

Need small silicon lab:

- Laboratory space (in hand?)
- Probe station (in hand)
- Wirebonder (in hand)
- Small "clean area"
- OGP (optical/touch-probe measuring & inspection)
- Granite table
- Full DAQ/Laser test stand



Small facility can serve both tracker and ECAL work at SLAC throughout R&D phase for ILC detectors

Summary

- 🔩 Silicon appears to be best answer to ILC tracking requirements
- 🔩 Some novel ideas needed: *KPIX is key*
- 🔩 *SLAC is leading development of tracker modules*
 - 🔩 Sensor design
 - 🔩 Mechanical design
 - 🔩 Readout design
 - 🔩 *Mounting design: interface with FNAL where support cylinders being developed*
- 🔩 Plan to prove concept with prototype modules in next 1-2 years
 - ⇒ *Small silicon lab needed to do any of this work at SLAC*
- 🔩 Need more simulation to optimize layout, design forward disks

SLAC playing a central role in ILC detector R&D efforts