ATLAS Tracker
Upgrade Projects

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DOE Review

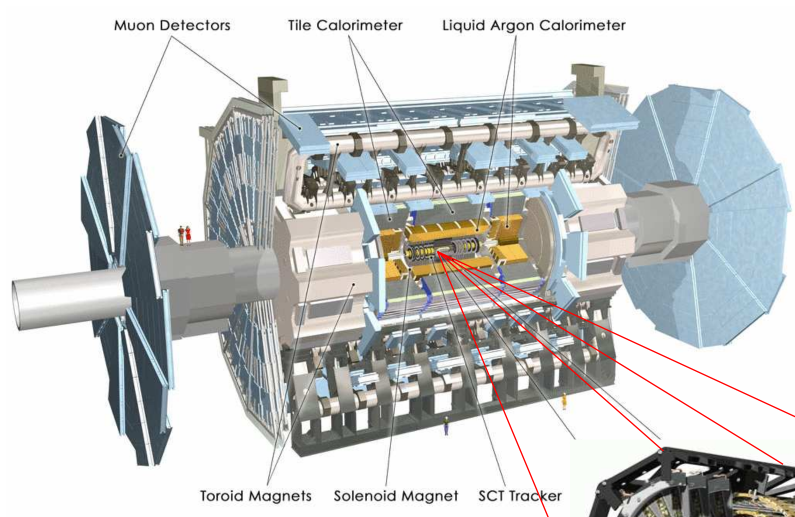
SLAC, 8 July 2008

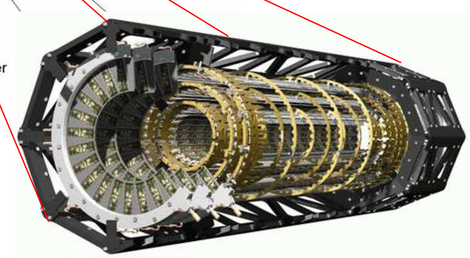
– Pixel data transmission

– SCT test stand

– Pixel test stand

Pixel Upgrade



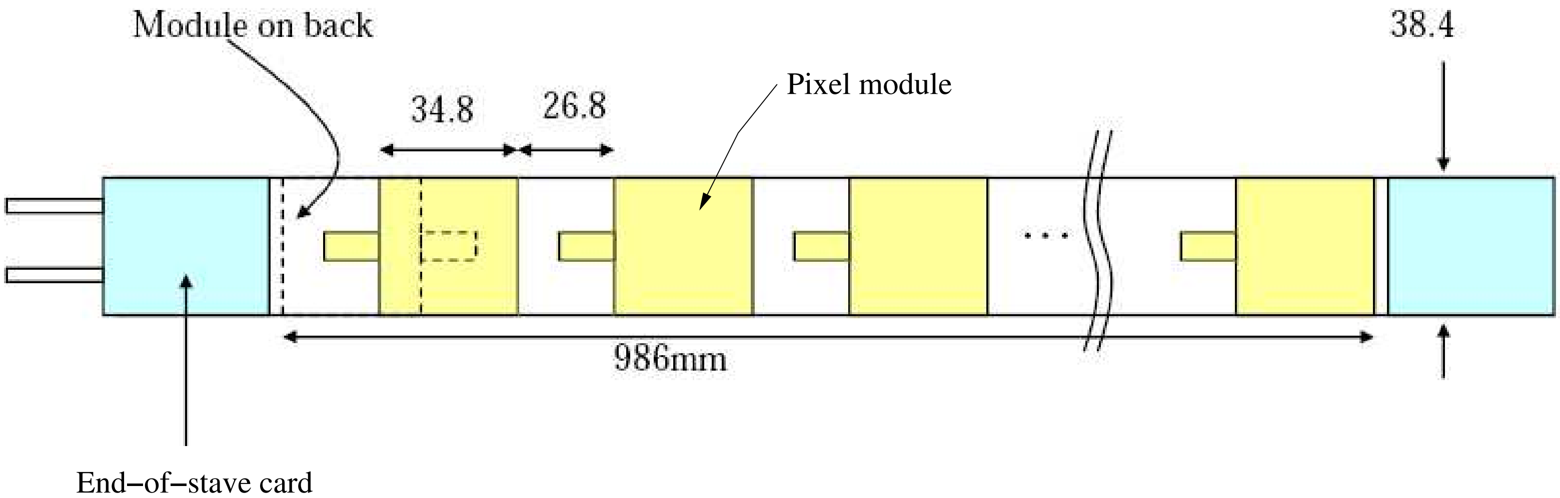


Why upgrade the pixel detector?

The SLHC luminosity target is 10^{35} cm^{-2}s^{-1}, 10 times that of LHC. To handle the increased event rates, background levels, and radiation dose the pixel detector will need:

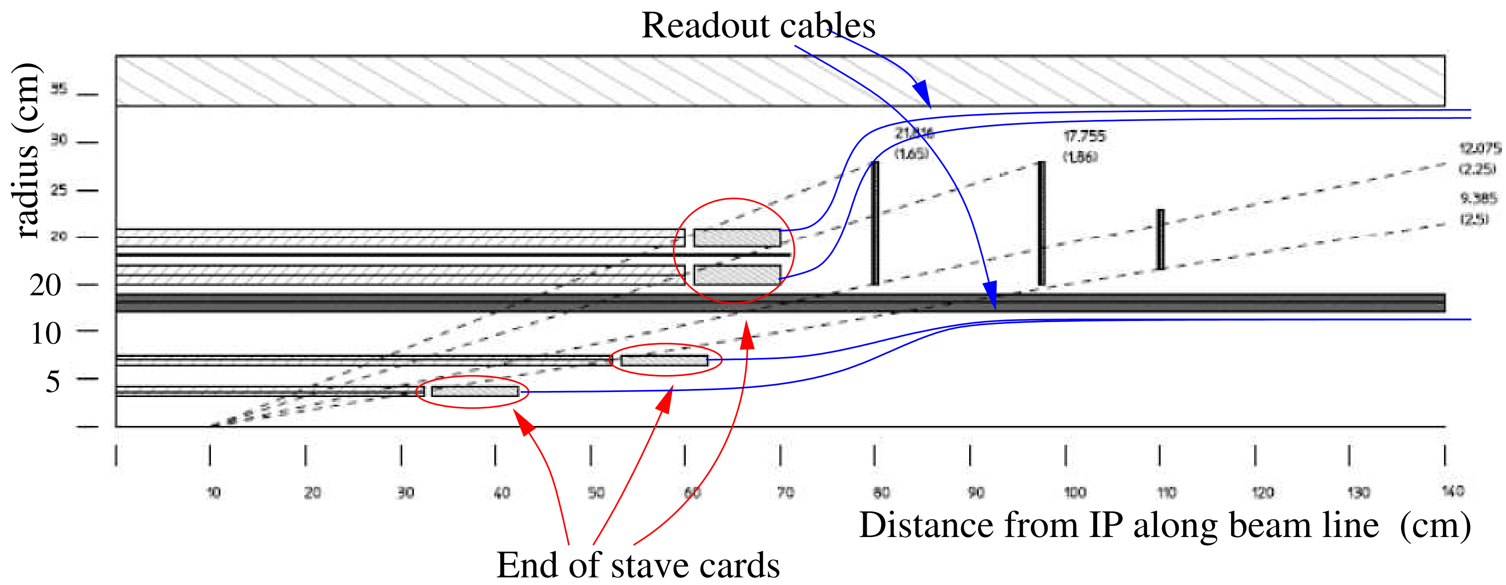
- Smaller pixels size for better granularity.
- Higher data bandwidth.
- Better radiation hardness for pixels and readout.
- Lower power consumption and better cooling.

SLHC Pixel "Stave" Design



- The pixel sensors are bonded directly to the readout chips.
- The chips are arranged on modules, 4 per module for the outer layers, 2 for the inner layers.
- In the barrel all modules of equal ϕ are attached to a support stave.
- The data for the chips of each half of a stave is read out by a super module controller at the end of the stave.
- The supercontroller serializes the data and sends it off the detector.
- The data rates for the innermost layers can be up to 9 GBits/second.

Data Transmission



- In some of the layouts for SLHC the innermost layer is only 3.5 cm from the beam.
- At this radius the yearly dose will be hundreds of Mrads.
- Because of assembly constraints the readout cables have to be routed at low radius.
- Optical fibers (used in ATLAS now) would not survive at this dose.
- Can coaxial cable be used to transmit the data over 4 - 6 m to a place outside the high radiation area to interface with optical fibers?

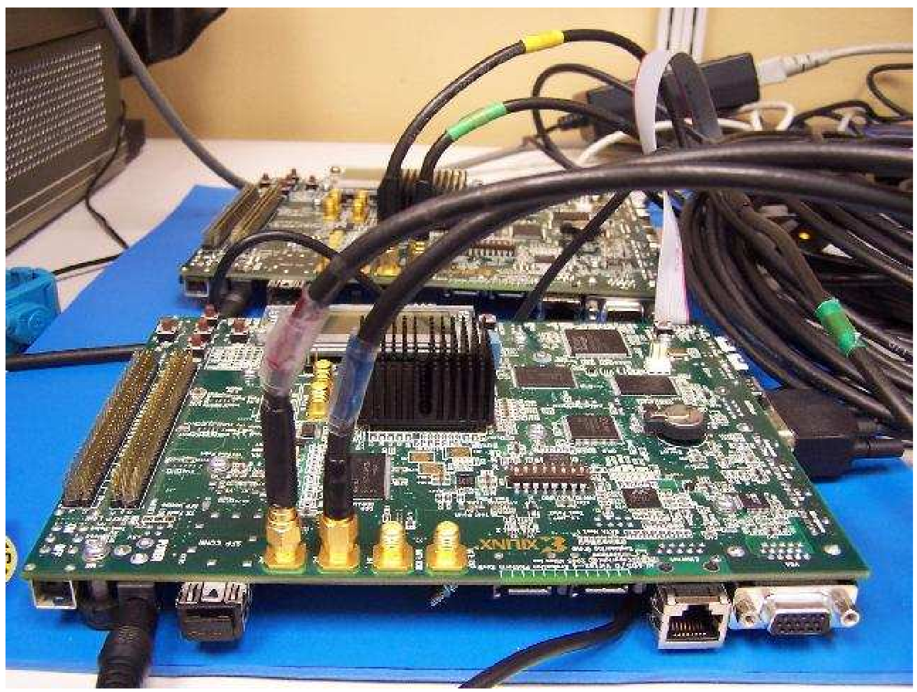
Data Transmission R&D at SLAC

SLAC (Dave Nelson, Su Dong, M. K.) is working on R&D on Gigabit rate transmission between the stave and the optical fiber link. This includes:

- **Coaxial cable:**
  - What rates can be achieved?
  - Which type of cable works the best?
  - How much material does the cable add to the pixel detector?
  - Is there coaxial cable that is sufficiently rad hard?
- **Transmission technology:**
  - Which electrical standard works best (single ended, differential, one or two coax cables per line)?
  - Do we need transmission enhancements like bit encoding and pre-emphasis?
- **Integration:**
  - How can the tranceiver be implemented in a rad hard ASIC?
  - Design a serializer to interface with the tranceiver in the ASIC.
  - How does the cable get attached to the board?

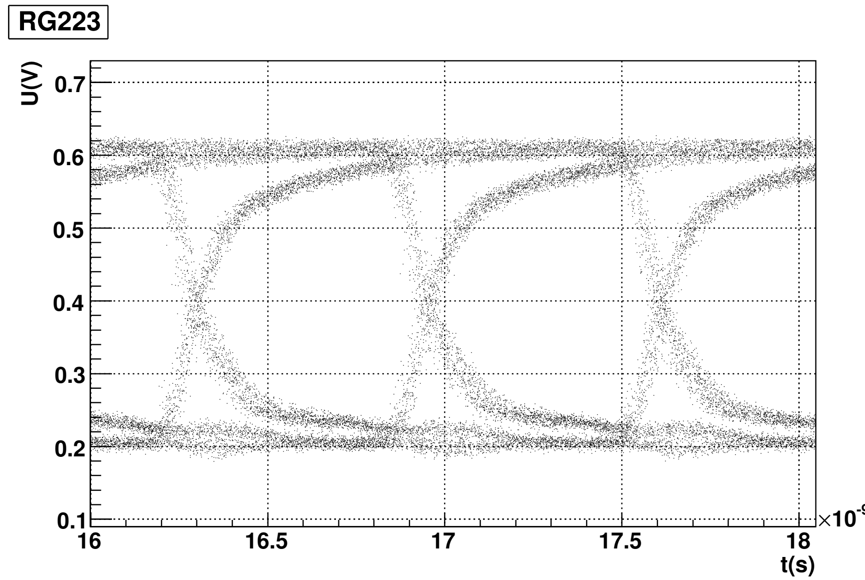
Coax Cable R&D

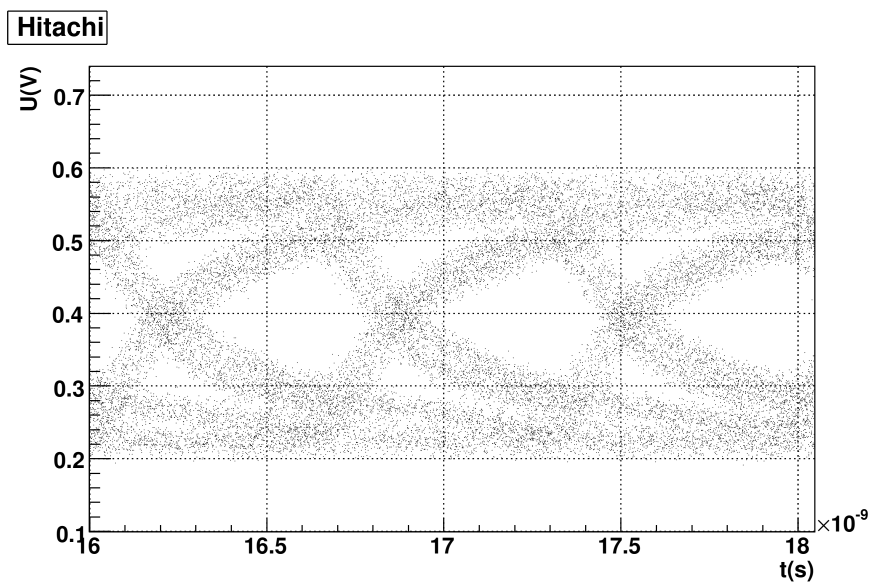
- Test cables of different sizes and materials.
- Use a random bit generator to look at the signal on the scope.
- Use a network analyzer to understand cable losses.
- Use a bit error rate tester to measure actual data transmission rates.
- We use the Xilinx 405 test board with RocketIO transceivers and a bit error rate test design:

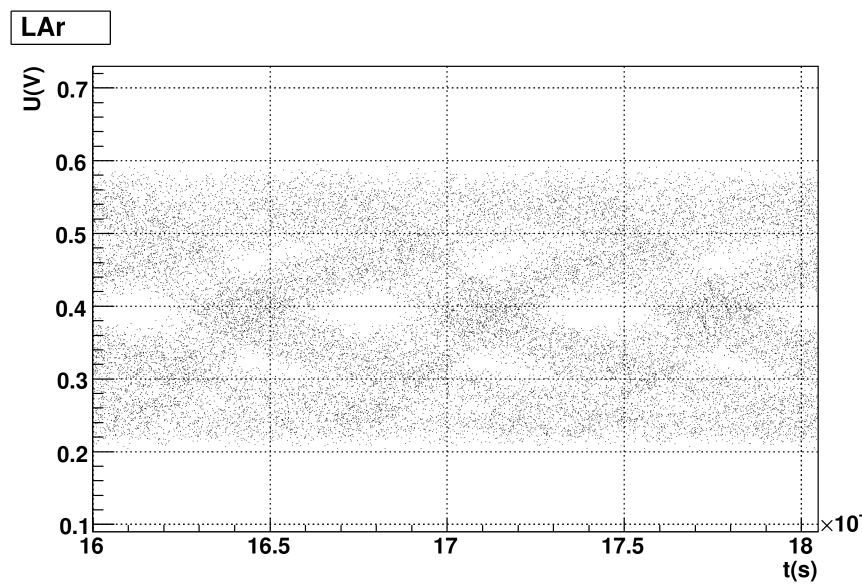


Eye Patterns

- Bit rate is 1555 Mbit/second.
- Right plot: RG223 (5 mm, polyethylene dielectric).
- Lower left plot: Hitachi (1.2 mm, Teflon dielectric)
- Lower right plot: ATLAS Liquid Argon Calorimeter cable (1.2 mm, Kapton dielectric).

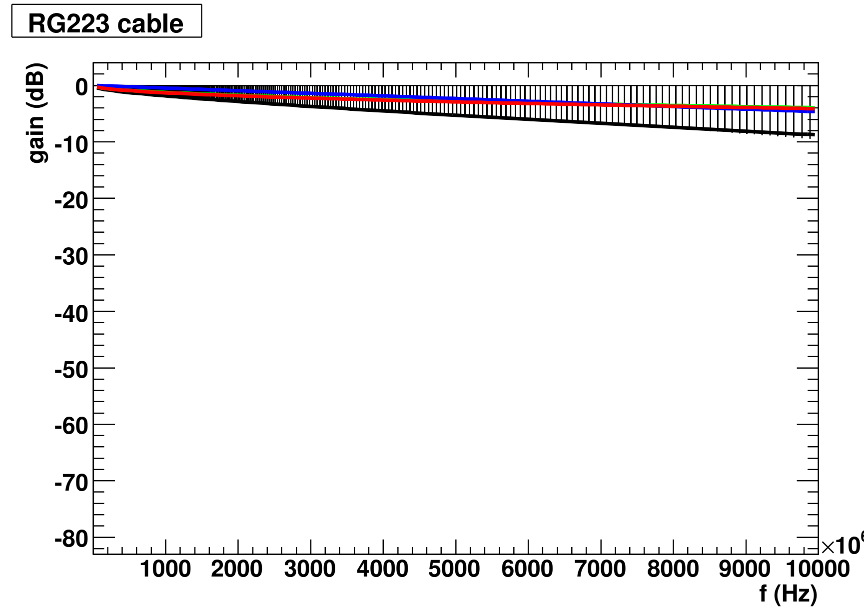


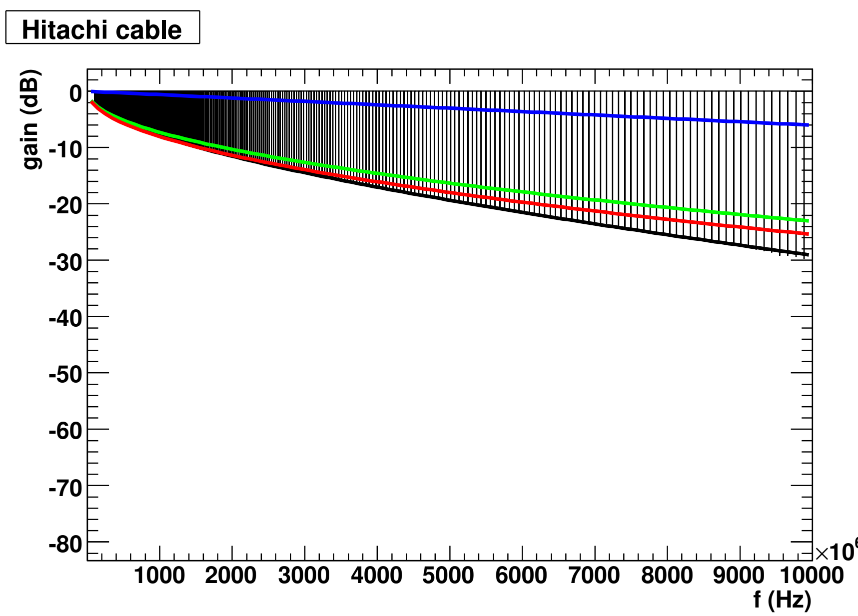


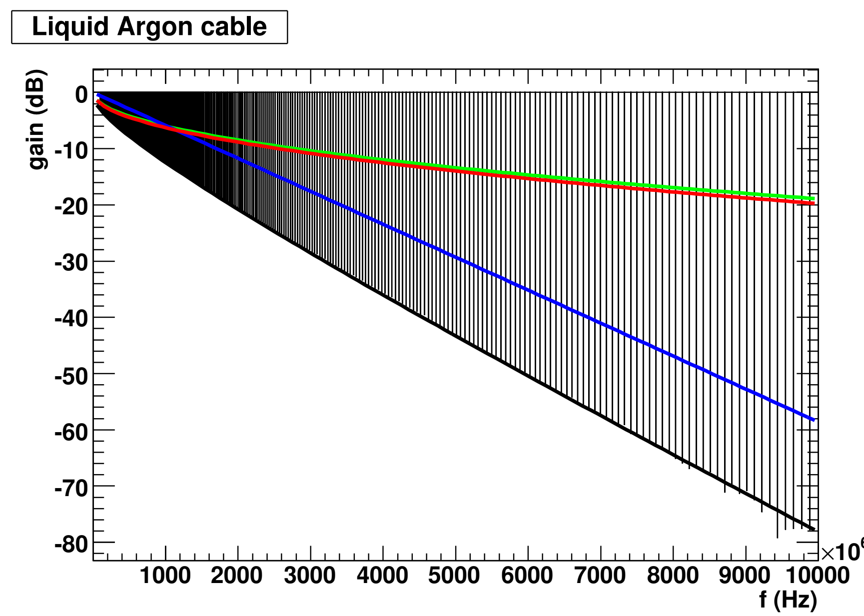


Understanding coax losses

- Measured with a network analyzer.
- Histogram: Data
- Black: Fit to $a_0 + a_1\sqrt{f} + a_2 f$
- Green: Metal loss $\propto \sqrt{f}$
- Red: Predicted metal loss
- Blue: Dielectric loss $\propto f$



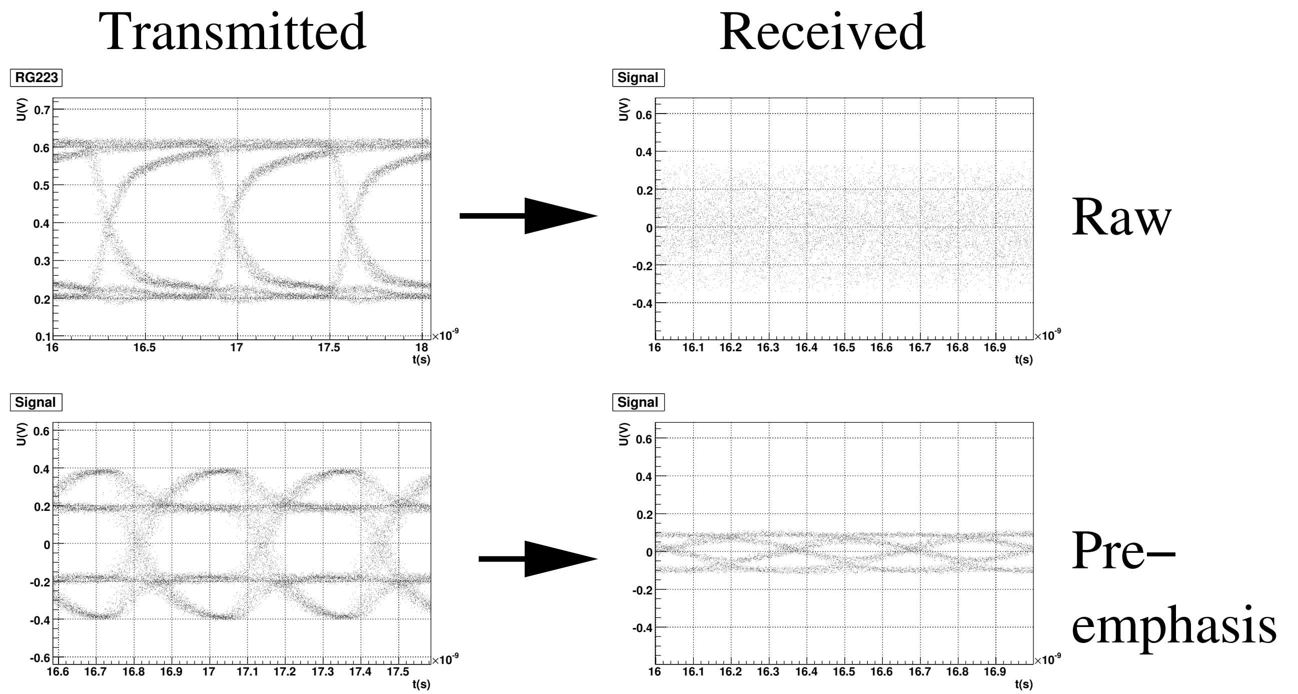




Signal enhancements

Pre-emphasis:

- Pre-emphasis creates an overshoot at each signal edge.
- This widens the "eye" of the signal.



Bit encoding:

- 8B/10B or 64B/66B encoding can be used.
- 8 (64) bits are mapped on 10 (66) bits for transmission.
- This avoids long sequences of only 0's and only 1's.
- Reduces bandwidth requirements.
- Better DC balance.
- Easier clock recovery.

Rate Measurements

- The table shows the highest rate with no errors after 10^{11} or more transmitted bits. (MBits/sec).
- Test frequencies are quantized by clock multiplication/division.

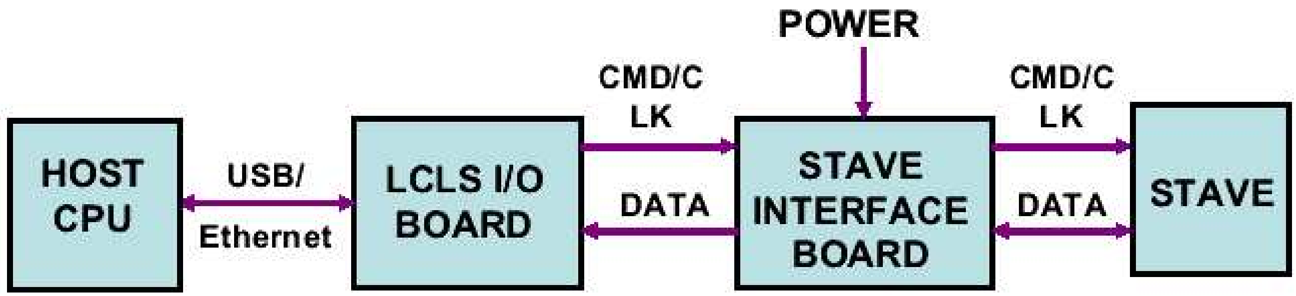
Cable	Raw	Emph/Eq only	8B/10B & Emph/Eq
4 m RG223 d=5 mm	3110	6220	9952
4 m Hitachi d=1.2 mm	1555	3110	6220
4.3 m LAr d=1.2 mm	?	3110	4095

- Test was done on coax pairs in the CML standard.
- d is the outer diameter of the cable.
- "?" means less than 1555 MBits/sec.
- The max rate for 6 m LAr cable is 3.1 GBit/s.

Next Steps

- Design a custom cable with good transmission and a low amount of material.
- Calculation predicts about 0.1 % of a radiation length per coax cable pair and stave (Up to 3 pairs may be needed).
- Test different transmission types (differential signal on one cable, single-ended signal).
- Do a radiation test on dielectric (planned for July at LANL).
- Investigate connectors.
- Design an ASIC to implement our own transceiver in rad-hard technology.

SCT Test Stand



- SLAC (D. Nelson) is designing a test stand for the silicon strip detector.
- The present SCT test stand is not fully adequate:
  - Too slow.
  - Not flexible enough to accomodate future readout development.
  - Proprietary hardware/software (National Instruments/Lab Windows).
- Features of the new test stand:
  - Fast histogramming implemented in FPGA.
  - USB based instead of VME.
  - Linux-compatible.
  - Electrically robust.
- The design of the new test board is complete.
- FPGA design and test software to be done.

Pixel Test Stand

What is the need for a new pixel test stand?

- The current test stand can only test the present generation of chips.
- It can only test one module at a time.
- It has a complicated setup (VME crate, National Instruments controller, Lab Windows, Microsoft Windows).

We (D. Nelson, Su Dong, M. K.) plan to design a new test stand at SLAC with the following features:

- Compatible with the present and with the new generation of readout chips.
- Can test a single module or a full stave.
- Can test several modules in parallel.
- USB based instead of VME.
- Linux-compatible.
- Fast histogramming implemented in FPGA.

Next Steps

- As a first step we have set up an existing "TurboDAQ" pixel test stand at SLAC.
- The TurboDAQ test stand will serve as a reference and for comparison of the results and the performance.
- We plan to use a similar Xilinx based technology for the new test stand as in our new SCT test stand.
- In a first phase we will reproduce the calibration results for the present generation chips.
- Next we will make the test stand work with the new generation of chips which is expected to come out next year.
- Finally the test stand will be made compatible with the to-be-designed stave supercontroller.

Summary and Outlook

Data Transmission:

- High rate transmission of pixel data is a crucial part of the pixel detector upgrade.
- This project is under active development at SLAC.
- From the initial R&D this looks like Gigabit rate transmission through coaxial cable is feasible.
- Our plan for the data transmission includes the design for coaxial cables, connections, and a serializer-transceiver ASIC.

Test stands:

- An FPGA based test stand for the SCT is under development.
- Work on a pixel test stand for the next generation of readout chips is starting.