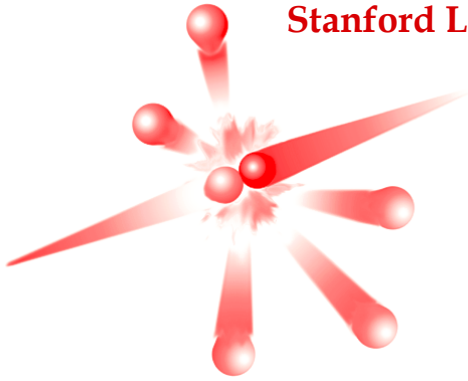**Stanford Linear Accelerator Center**

INTEGRATING TIMING WITH REAL-TIME DATA ACQUISITION AND CONTROLS

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Timing System Functions

- Provide RF phase reference (fine triggers).
- Sequence events within a pulse (coarse triggers).
- Vary sequence from pulse-to-pulse; each pulse is either selected from a pre-established repertoire or *sui generis*.
- Degrade beam intensity/rate under abort or machine protection conditions.
- Synchronize activities on a given pulse or set of pulses; trigger on abort/MPS events.
- Report errors in clock, fiducial, and data streams required to accomplish above tasks.

Pre-SLC LINAC

- Master drive line to phase klystrons.

- Master trigger line to generate a pulse.

- No controlled pulse-to-pulse variation.

- No common method for programmable sequencing within a pulse.

- No computer networks.

SLC Timing/Control System

- Merge MTL with MDL; put fiducial on 476 MHz phase reference & derive 119 MHz clock.

- PDU provides common method for sequencing within a pulse; sequence is selected by "pp" on a pulse-to-pulse basis.

- PNET distributes "pp" and other pulse-to-pulse data at 1 megabit/second via unidirectional broadcast from MPG.

- SLCnet carries front-end data acquisition and control functions at 1 megabit/second, including common PNET error reporting function, to front end Multibus-I micros.

- State-of-the-art network bandwidth for multi-kilometer LAN coverage in early 1980s.

Front-End Upgrade Project

- Replace each Multibus-I micro by PC in MCC computer room plus intelligent Front-End CAMAC Controller at micro's old location.

- FECC-3 implementation is SOPC with embedded PPC405 at 250 MHz; 125 megabyte/second serial fabric on gigabit Ethernet physical link to special NIC at PC (64-bit/66 MHz PCI board).

- Fabric provides noise-tolerant network link with prioritized, circuit-switched support for pattern distribution, real-time streaming data acquisition & loop closure, and non-critical networking.

Adding Timing Support to Network Fabric

- Network bandwidths have increased by 3-4 orders of magnitude since SLC timing architecture was designed.

- Derate fabric byte clock frequency from 125 to 119 MHz.

- Derive sector 119 MHz PDU clock from fabric byte clock instead of from MDL fanout (FIDO).

- Carry 119 MHz fiducial in fabric cell header.

- Remove all timing support from temperature stabilized MDL replacement and use only for phase reference; avoids headaches arising from conveying fiducial along with stable phase.

Timing Stabilization

- First-order temperature stabilization to fiducial timing provided by running fabric fiber in same bunch with phase reference; not good enough for sub-picosecond MDL phase accuracy but far better than one 8 ns tick at 119 MHz.

- Further stabilization from 1 Hz feedback loop closed by vernier delay on 119 MHz output; vernier data in cell header; error signal from phase comparison with stabilized MDL reference phase.

2nd Generation Link

- All traffic divided into 608 byte cells.

- 320 bytes of user data (real-time, non-real-time, pattern, no-op/zero); 32 bytes of hardware header; 256 bytes of error correction code.

- Cell requires 4.864➔5.109 microseconds; can withstand 128 consecutive bytes or > 1 microsecond of lost data in that time.

- Klystron modulator pulse is > 5 microseconds wide with < 1 microsecond rise and fall times; can survive loss of all data on both rising and trailing edges of a single modulator pulse.

2ⁿᵈ Generation Link II

- If uncorrectable errors, hardware timeout and retransmission of all lost cells; 100 microsecond (20 cell lengths) typical timeout length.

- Hardware flow control for 16 real-time receive buffers and 16 non-real-time receive buffers.

- No start-of-message sequences to be corrupted by noise after initial turn-on.

- Hardware header supports remote manipulation of initialization register; local and remote hardware error counters.

Link Header Format

- All fields 16 bits unless noted.
- Command :
  - 4 bits - destination buffer number;
  - 1 bit - first cell in buffer;
  - 1 bit - last cell in buffer;
  - 2 bits - cell type (Pattern/R-T/N-R-T/NOP);
  - 1 bit - remote initialization register write enable;
  - 7 bits - unused.
- Offset in buffer to end of cell, i. e. cumulative buffer length including this cell (64 byte chunks).

Link Header Format II

- Remote initialization register write data (32 bits).

- 16 non-real-time receive buffer available bits (backpressure flow control).

- 16 real-time receive buffer available bits (backpressure flow control).

- 16 non-real-time receive buffer filled handshake bits.

- 16 real-time receive buffer filled handshake bits.

Link Header Format III

- Outgoing cell sequence number.
- Next expected incoming cell sequence number.
- Multiple cells acknowledged event count.
- Received cell out-of-sequence error count.
- Timeout error count.
- 8B/10B decoder error count.
- Reed-Solomon corrected error count.
- Uncorrectable Reed-Solomon error count.
- Outgoing and incoming versions of last 8 counters readable from PPC405.

Integrated Architecture Details

- Transport TCP/IP service on non-real-time circuit.

- Run EPICS (under VxWorks/RTEMS?) on second embedded PPC405 processor in each non-FECC3 SOPC FPGA on 119 MHz fabric.

- Interpret remote initialization register write data as generalized link maintenance data.

- Retain existing load enable bit for this data; add two bits to select destination (fiducial offset from start-of-cell/vernier delay/link maintenance register); or, enable can be non-zero destination.

- Load fiducial offset generates fiducial in *next* cell.

Flavored Fiducials

- Fiducial marker in cell header carries 32 bits, but only 10 needed for fiducial offset in cell (608 ticks long).

- Remainder can be used for last minute changes to pattern, especially levels of abort processing and MPS restriction.

- Example: divide 1k bit pattern broadcast into four 256 bit sections; use two bits in fiducial data field to select from among these patterns.

- Pattern broadcast becomes conditional roadmap of future pulsed activities.

LINAC Sector Plant

- Sector PC has two NICs for noise-tolerant fabric:
  - First NIC supports fabric with 125 MHz byte clock; connects to legacy CAMAC/BITbus plant via FECC3;
  - Second NIC supports fabric with119 MHz byte clock; initial connection is to SOPC controller implenting PIOP replacement and clock/fiducial generation for legacy PDU plant; new BPM controller to follow.

- 119 MHz fabric can fan out to other (i.e. non-PIOP) nodes via either a repeater in PIOP or a stand-alone fabric switching node.

- Possible direct connection from BPM controller to RF controller without going through sector PC.

PIOP Replacement Architecture

- Dual (triple?) processor SOPC FPGA with one PPC405 for real-time streaming data acquisition and a second PPC405 for EPICS control & configuration replaces all 9 PIOPs in a sector.

- Existing interlocks/hardware safety algorithm in dedicated hardware sequencer in FPGA fabric or third PPC405 with independent code (no RTOS?).

- Individual point-to-point 100baseT hardware link to each of 9 new PADs for streaming waveform acquisition (9@100baseT → 1@1000baseT).

MKSU Interface/Upgrade

- Individual point-to-point 100baseT hardware link to new controller board for each of 9 existing MKSUs.

- Supports streaming data acquisition from future solid-state modulators and their associated interlock systems.

- Does trigger need its own connection to actually get from PIOP to MKSU/modulator? Can we use arrival time of 100baseT message? Can we reserve channel/orchestrate traffic? 119baseT?

R&D Efforts

- Demonstrate ability to design with embedded PPC405 in FECC3; debug deferred until January.

- Investigate generation of BSPs and required hardware configurations for VxWorks/RTEMS, including use of Xilinx System Generator; mid-November to mid-December.

- Design & test dual-processor SOPC architectures; SBIR Phase I proposal due mid-January.

- TCP/IP on non-real-time fabric circuit in SBIR Phase II (2005).

Conclusions

- Phase accuracy requirements on MDL are far tighter than they were 20 years ago.

- Data communications bandwidths at level where integrating clock and fiducial into communications fabric instead of phase reference is simple now.

- Single fiber carries timing, sequencing, real-time data flow, and control/error reporting.

- Bandwidth to stream all pulsed waveforms from front end is cheap already; bandwidth to process all these data will become available with time.