Minerva: A Compute Capable SSD Architecture for Next-Generation Non-Volatile Memories

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Future System Architecture

IO access time $\approx$ nanoseconds! (read hit in L1, L2 caches)

1X latency

DRAM

>100000X latency

Disk

~1-100X latency

Memory Controller

I/O Controller

Cache (SRAM)

CPU

CPU

PCM

STTM

MRAM

Flash
Why Minerva?

• Growing demand for data-intensive applications
• Emerging non-volatile storage technologies are promising
  — Byte-addressable, DRAM-like latency & BW
• Limited External IO bandwidth
• Power efficiency
Minerva

• Based on moving computation close to data
• Moved data intensive computation to storage to avoid redundant data transfer between the host and the storage
• Huge power and performance gain for data intensive application
Minerva Architecture on BEE3

- **Host interface**
  - PCIe 1.1 x8 (2GB/s Full Duplex)
  - Scheduler

- **4.0GB/s Ring Network**

- **Storage Processor**
  - Mem Ctrl
  - Start Gap
  - 16GB DDR2

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