Strategies for pickup and noise suppression with different vertex detector technologies

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- The problem: $10^9$ signals being read in an electrically hyperactive environment
  - could produce a data deluge
  - contrast between different collider options (2) and detector options (at least 5)
- Reality check: 300 M pixels at SLD
- CCD-based detector at NLC (natural evolution)
- CCD-based detector at TESLA
- Other detector technologies at NLC/TESLA
CCD signal storage and sensing:

“Classic CCD”
Readout time \( \approx N \times M / F_{\text{out}} \)

Column Parallel CCD
Readout time = \( N / F_{\text{out}} \)
• Signal charge from MIP stored safely in buried channel of device

• During readout, charge is transferred to output node

• Classical Correlated Double Sampling (CDS):

  \[ \text{RESET/READ 1/TRANSFER/READ 2} \] (originally to suppress reset noise)

• Sparse data scenario permits faster (but equivalent) noise suppression:

  \[ \text{RESET/READ 1/TRANSFER/READ 2/TRANSFER/READ 3/} \ldots \]
In addition, Extended Row Filter (ERF) can suppress pickup:
SLD experience:

Without ERF, rate of trigger pixels would have deluged the DAQ system.

Readout at 5 MHz, during ‘quiet’ inter-bunch periods of 8 ms duration.
• For NLC, substitute bunch train for bunch
• Otherwise, as at SLD, and expect same strategy to work
• Can again wait many $\mu$s for beam-related pickup to die away
• CPCCD lends itself to required functionality in readout chip
• For TESLA, one enters uncharted waters
• Must read during most of 337 ns between bunches (17 samples at 50 MHz in CPCCD)
• Could cut to say 14 samples giving ~ 50 ns settling time. Will this suffice?

What will be the noise penalty due to pickup between samples N and N+1?
MOS transistor instead of JFET

A pixel size of ca. 20 x 20 µm² is achievable using 3µm minimum feature size.
DEPFET pixel matrix

- Read filled cells of a row
- Clear the internal gates of the row
- Read empty cells
• DEPFET enjoys same strengths as CCD regarding CDS
• However, ERF would slow down the readout correspondingly

[N samples before and after RESET would imply N-fold increase in readout time]

• Will ERF be more or less important at 50 MHz during the TESLA train than it was at 5 MHz at SLC? Also, the readout electronics is, in some senses, much more compact, both for CCD and DEPFET ...
Basic MAPS architecture at TESLA

- Strasbourg group – Marc Winter et al
- ‘Transverse’ readout to satisfy the 50 μs requirement
- SAMPLE/RESET at 50 μs intervals
- Should be OK for readout noise, but could be catastrophic for pickup from intervening 150 BXs
- Possible way out: Could do SAMPLE/RESET/SAMPLE within one BX, at 50 μs intervals
- This would strongly suppress pickup while sacrificing the suppression of reset noise. Tolerable for $C_{\text{NODE}} < \text{approx} 10 \text{ fF}$
- Could also (at expense of readout time) implement CCD-like ERF if required
LCFI

[Diagram showing a waveform and annotations]

- 333ns
- 50us (12.5Bx)
- N
- N+1
- Will latter part of inter-bunch period be clean enough?
  - May be OK
- First parallel reset of all pixels
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12
FAPS or FAPS(CAP) concept: Renato Turchetta

- Flexible APS permits storage of 20 samples during train
- Readout of above-threshold pixel hits and their neighbours proceeds at leisure in the 200 ms between trains
- This will permit ‘longitudinal’ readout, with benefit to material budget
- However, CDS options are no different than for MAPS
New concept: FAPS (CCD)

- MIPs which hit the storage register (<10% area) leave a small spurious signal – easily handled by software

- Lessons being learned about CCDs with reduced clock amplitude (e.g. without barrier implants) will feed directly into this design concept

- Increasing availability of mixed CCD/CMOS technology at a few foundries

- Implementation architecture:
• Column-pair readout of sparse data (analogue signals to ADCs at ends of ladder)

• Manufacturability would require not only mixed technology, but also large area precise stitching, etc

• Could provide the ultimate in pickup immunity, but will this be necessary?
CONCLUSIONS

- Pace of development of silicon pixel devices {CCD, MAPS, FAPS (CAP), FAPS(CCD), DEPFET, SOI, HAPS, …} is breathtaking

- High level of pickup immunity can surely be engineered into some or all of these architectures

- If at end of this year, we have a warm machine, we can relax and focus mainly on other criteria

- If TESLA, suggest producing a serious BDS mockup to simulate pickup effects

- In either case, expect surprises from \(10^9\) pixels in the LC environment, so it’s probably wise to back contrasting technologies for the (assumed) two detectors, in order to spread the risk

- At SLD, we were lucky in being able to retro-fit the ERF. Inadvisable to assume this luck will hold, in the unknown territory to be explored next time …
The diagram illustrates a process involving a Tesla IR train with a TDEL (time delay element). The correlation double sampling (CDS) is indicated on the right side of the diagram.

A section labeled 'classical CCD' suggests a signal related to NLC (normalized long chain). The signal S1-S2 is free of reset noise and slow pickup for fast pickup protection.

The diagram also includes an ERF (extended row filter) notation, emphasizing the importance of signal processing.

Below, a table shows comparisons between S2-S1 and S2-S1', with checkmarks (✓) indicating when certain conditions are met. For S2-S1, reset noise is present, while slow pickup noise is absent. For S2-S1', slow pickup noise is present, and reset noise is absent.