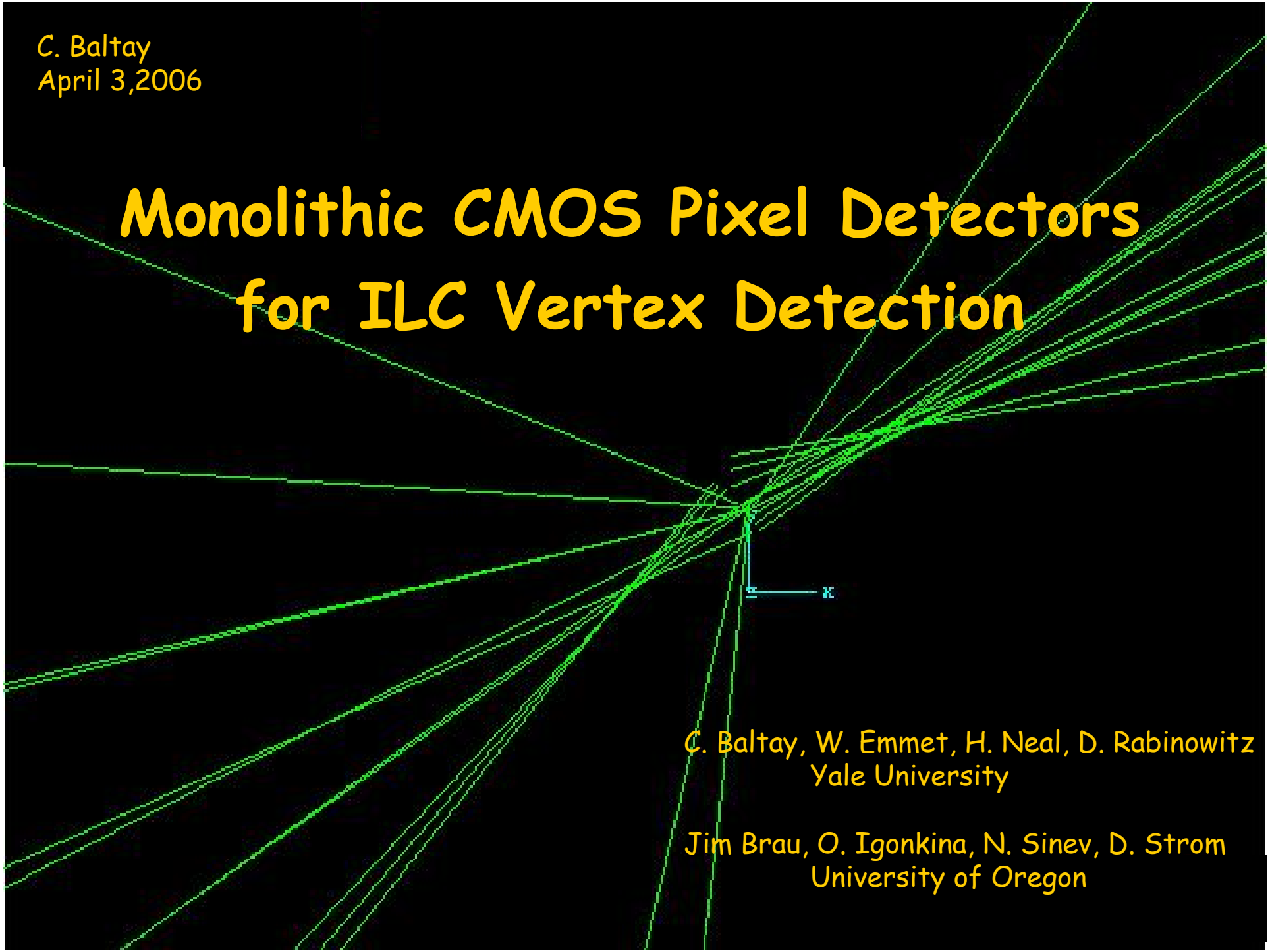
C. Baltay
April 3,2006

Monolithic CMOS Pixel Detectors for ILC Vertex Detection



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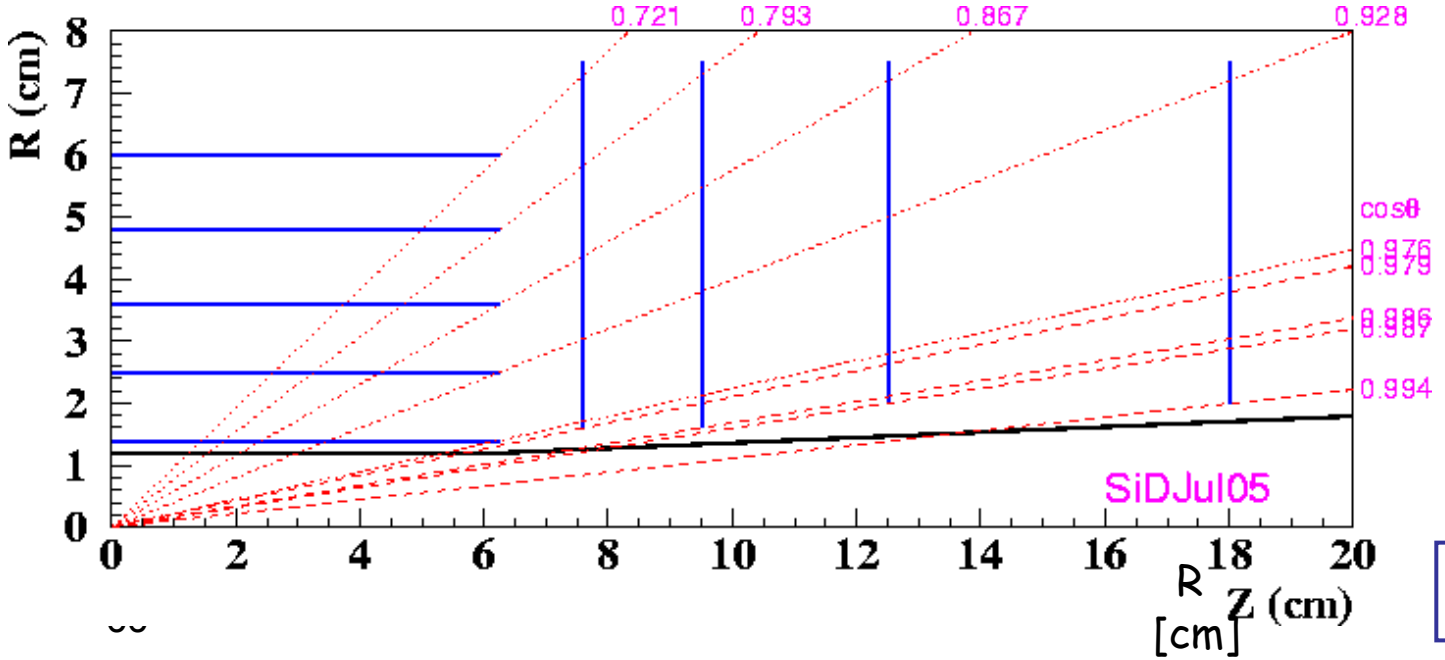
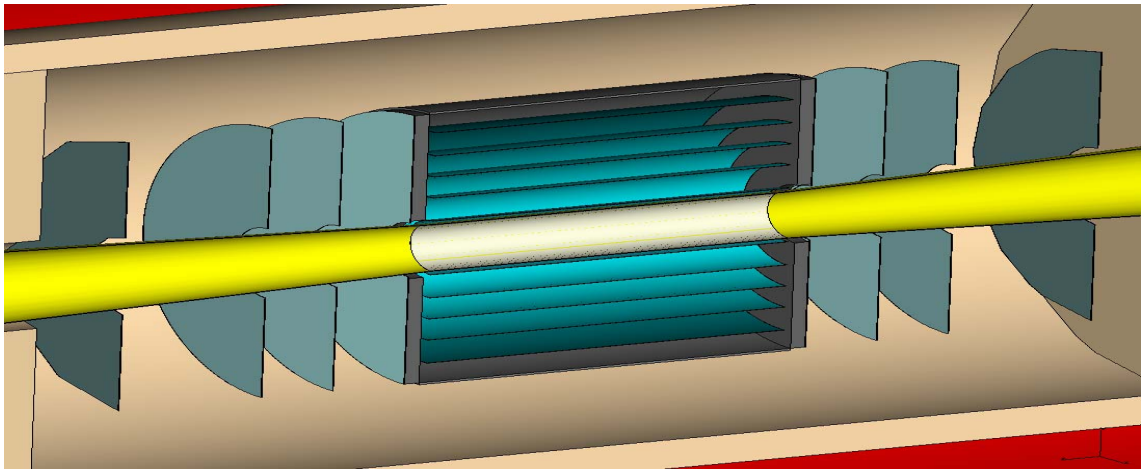
SiD Vertex Detector Layout



5 barrel layers
4 end disks

5 Tesla



SiD Vertex Detector

- BARREL
  - 100 sensors
  - 1750 cm^2
- FORWARD
  - 288 sensors
  - 2100 cm^2

Table I: CMOS Detector Barrel Configuration

Layer	Radius (cm)	Total Length (cm)	No. of Chips	Chip Size (cm^2)
1	1.4	12.5	12	12.5×1.2
2	2.5	12.5	24	12.5×1.2
3	3.6	12.5	20	12.5×2.2
4	4.8	12.5	20	12.5×2.2
5	6.0	12.5	24	12.5×2.2

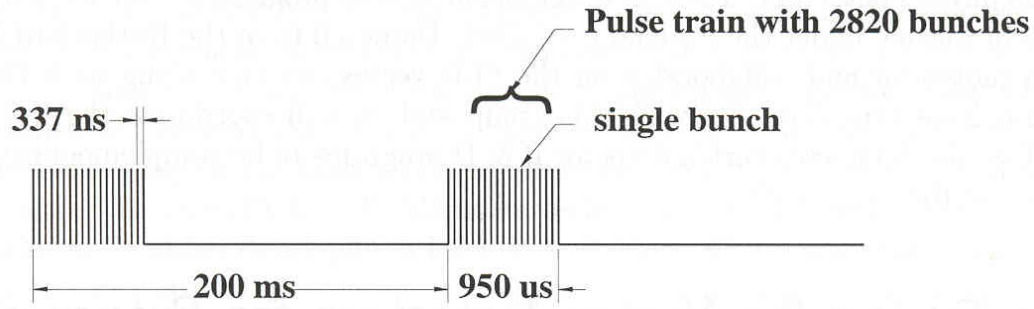
Table II: CMOS Detector Forward Disk Configuration

Annulus	Inner Radius (cm)	Z (cm)	No. of Chips	Chip Size (cm^2)
1	1.6	7.6	24	1.5×0.9
	3.1	7.6	24	4.4×2.2
2	1.6	9.5	24	1.5×0.9
	3.1	9.5	24	4.4×2.2
3	2.0	12.5	24	1.1×0.9
	3.1	125	24	4.4×2.2
4	2.0	18.0	24	1.1×0.9
	3.1	18.0	24	4.4×2.2

Consider Typical Chip of 12.5cmx2.2cm

Time Structure for the TESLA Design

Assume this design for the ILC for Now



Background Calculation:

At 1.5 cm from Interaction Point with 3 Tesla field expect

0.03 hits /mm^2/bunch crossing

Will use this number for the entire detector

Conventional CCD's Not Well Suited for This Application

- Consider SLD type CCD's with 20μ x 20μ pixels
  - 22 mm x 125 mm = 2750 mm^2
  - with 6.9 x 10^6 pixels/CCD,16 bits per pixel=110x10**6 Bits
- Readout time at 50 MHz is 2.2 sec
  - Need to divide CCD into ~20, readout sections,then

➔ Can readout in 200 msec between pulse trains

- Occupancy, integrating over 2820 bunches in a pulse train
  - 0.03 hits/mm^2/bunch x 2820 bunches x 3 pixels/hit
    - = 250 pixels hit/mm^2
  - or 10% of the pixels have a hit (occupancy)
- SLD Experience – occupancy of 10^{-3} or 2.5 hits/mm^2 are maximum we could handle!

➔ Occupancy too high by factor of ~ 100!!

Monolithic CMOS Pixel Detectors

➔ What are they?

- New CMOS technology makes pixels as small as 10 μ x 10 μ possible
- Each pixel has its own intelligence (electronics) under the pixel
- Unlike CCD's, all pixels are NOT read out in a raster scan
- Reads out x,y coordinates only of pixels with hit (i.e., exceeding an adjustable threshold) at 50 MHz
- Monolithic design – photosensitive detector pixel array and read out electronics for each pixel on the same piece of silicon – can be quite thin (less then 50 μ)

➔ Advantages over CCD's

- Significantly faster read out. Typical occupancy of vertex detector at e^+e^- collider ~ 10^{-3}
  1000 times faster read out! (Read only hit pixels!)
- Potentially more radiation hard
- Small 10 μ x 10 μ pixels allow good resolution

➔ Advantages over hybrid pixel devices used at the LHC

- Monolithic – can be much thinner than hybrid devices
- Do not need bump bonding of pixel detector to electronics layer
- Allows much smaller pixels

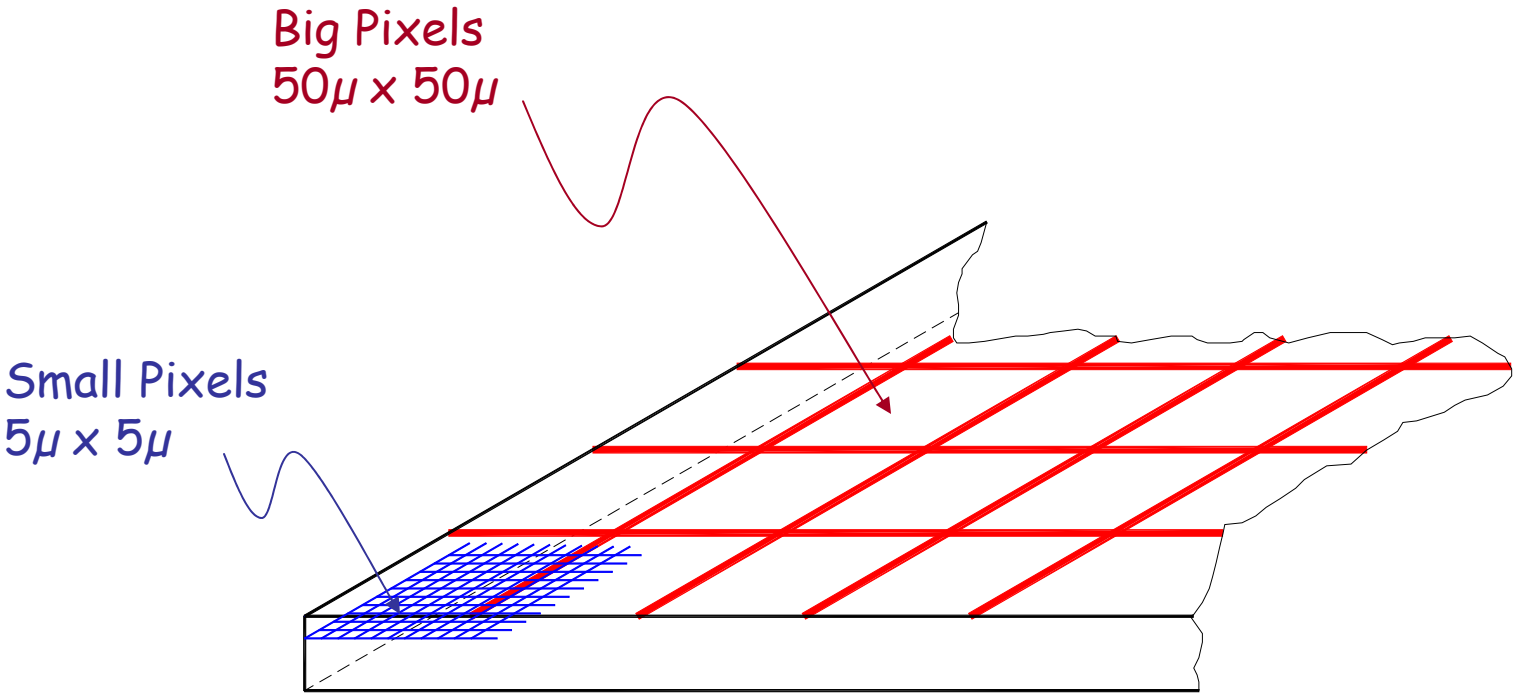
Conceptual Design

- During the past year, working with SARNOFF we developed a conceptual design that:
  - we believe will work for an ILC Vertex Detector
  - that SARNOFF believes they can build.
- Plan to integrate over pulse train and readout during 200 msec between trains to avoid EMI (Electromagnetic Interference) during train.
  - Occupancy would be too high
  - BUT – for each hit, readout x,y, intensity, AND time of hit (time to better than 300 nsec precision effectively tagging each hit with its bunch crossing number)
  - In analyzing Vertex detector data look only at hits which occurred in the same single bunch crossing

➔ Occupancy ~ 10^{-6} or 0.03 hits/mm^2!!

First(now obsolete) Design

Hierarchical Design with Macropixels and Micropixels



Two active particle sensitive layers:

Big Pixels – High Speed Array – Hit trigger, time of hit
Small Pixels – High Resolution Array – Precise x,y position, intensity

Background Hits Dominate in Vertex Detector

1. Events of interest are relatively rare – much less than 1 per second. Hit rate in Vertex Detector is dominated by background.
2. Recent detailed calculations confirm the background estimate we have been using

   0.03 hits/mm^2/Beam Xing

3. There is still a considerable uncertainty about the level of this background.
   a) It is a difficult calculation to begin with.
   b) The Collider design has been chosen but details of the design are still being worked on. The background may depend on these details.

The Macropixel Array is Critical

The size of the Big Pixels (previosly 50 μ x 50 μ) limits the tolerance to higher backgrounds. It is therefore important to work towards reducing the size of the Big Pixels:

a) Reducing the Big Pixel size to 10 μ x 10 μ would allow the detector to be much more tolerant to high backgrounds.

b) With the Macropixel Array (Big Pixel size) down to 10 μ we would not need the micropixels and could simplify the design to a single layer of "Macropixels" with time information, and could do without analog information (digital readout!)

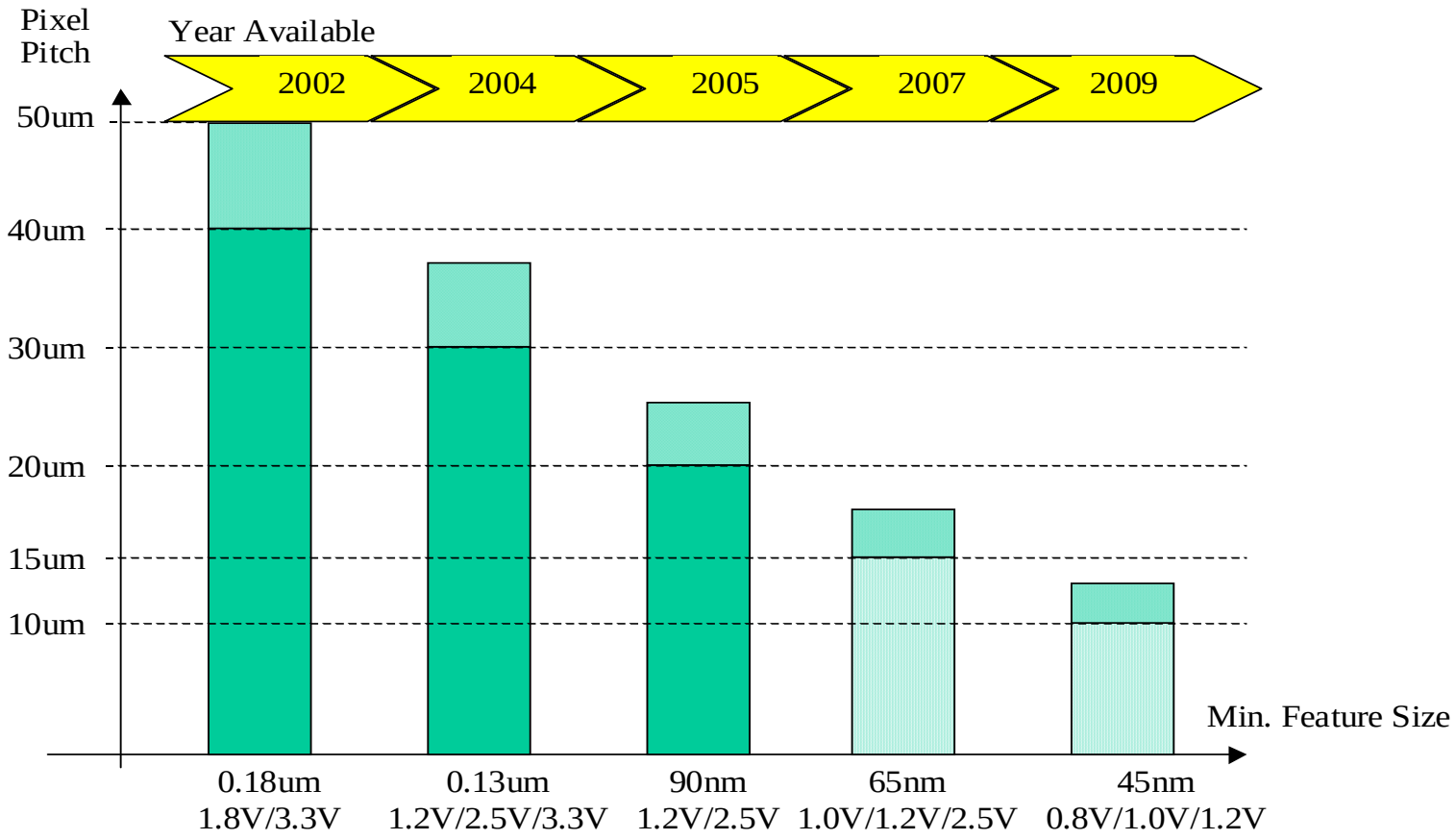
What Limits the Macropixel Size

How small can we make the Big Pixel and still store the hit time information of up to 4 hits/pixel

a) Area needed with present technology (0.25 μ) for:
   - Comparator/counter/latch, etc., circuit
   - Storage of up to 4 hits, i.e., 13 bits 4 deep

b) Process Technology – how does pixel size scale as process technology goes from 0.25 μ to .13 μ to . . .?
   - What do you need to go to 10 μ x 10 μ pixels?
   - Can you estimate the progress of this technology
     - What's available today?
     - Much more interesting – what will be available ~ 5 years from now when we need to fabricate the actual devices?

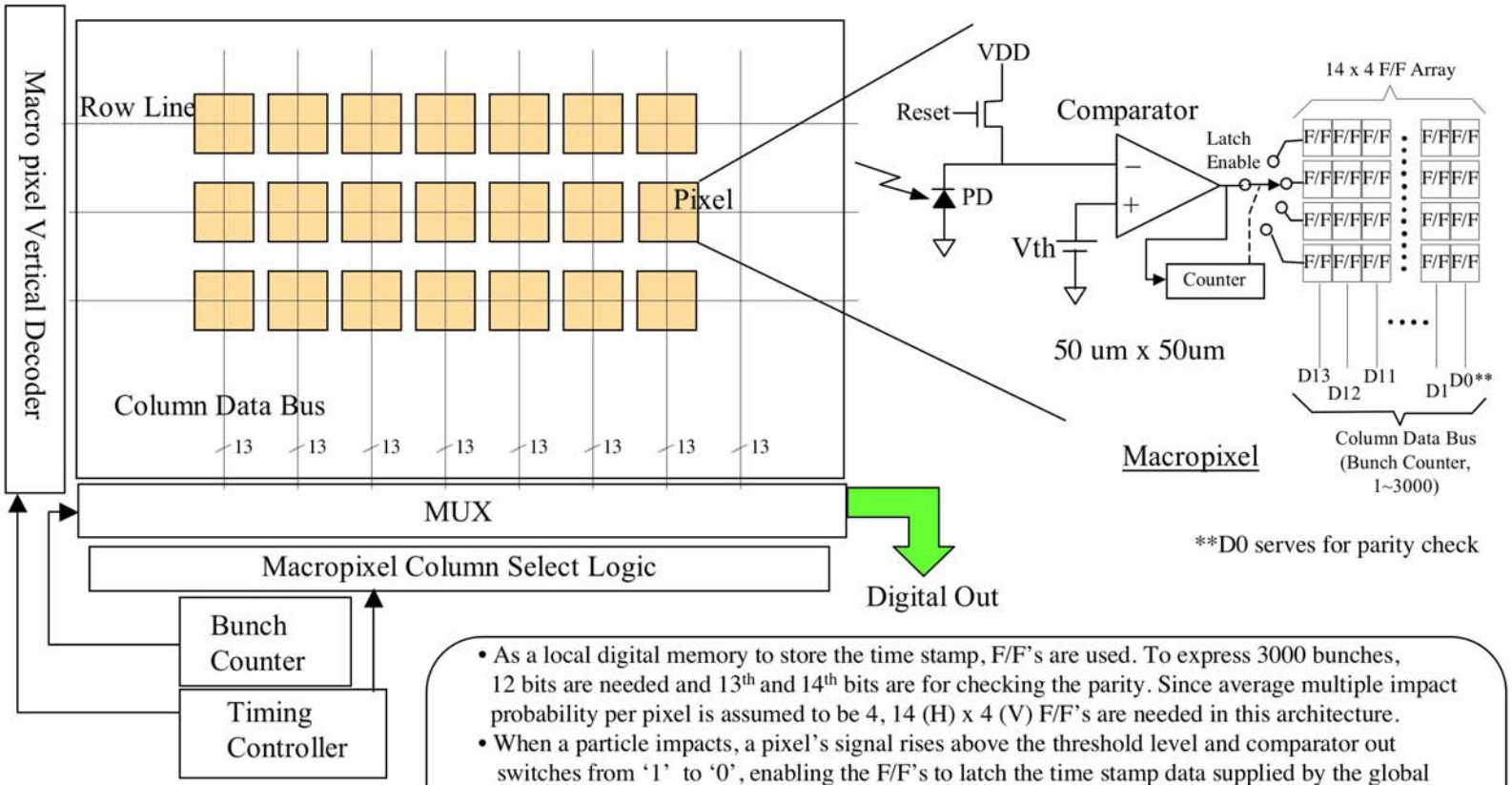
Technology Roadmap: Macropixel size estimation vs. Mixed-signal Process Technologies



Current Design

- Monolithic CMOS Process
- Single Layer of 10micronx10micron Pixels
- Detect Hits above adjustable Treshhold
- Store time of Hit, up to 4 hits/pixel
- Integrate over Bunch Train, Readout during 200 msec between trains
- Digital Readout(no Analog)

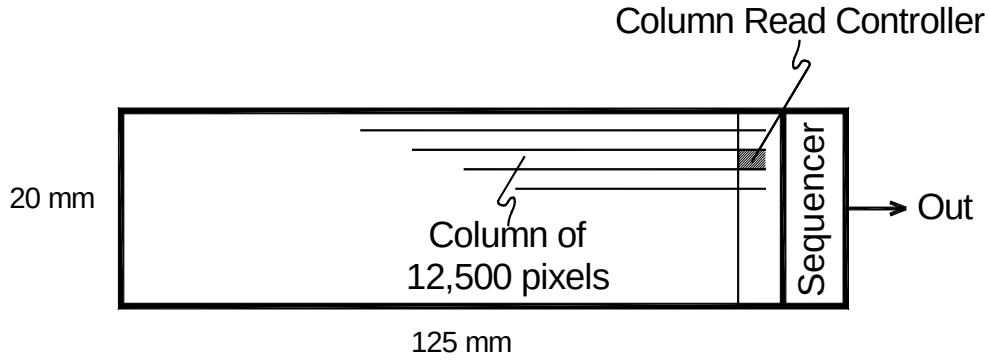
Macropixel Array Architecture



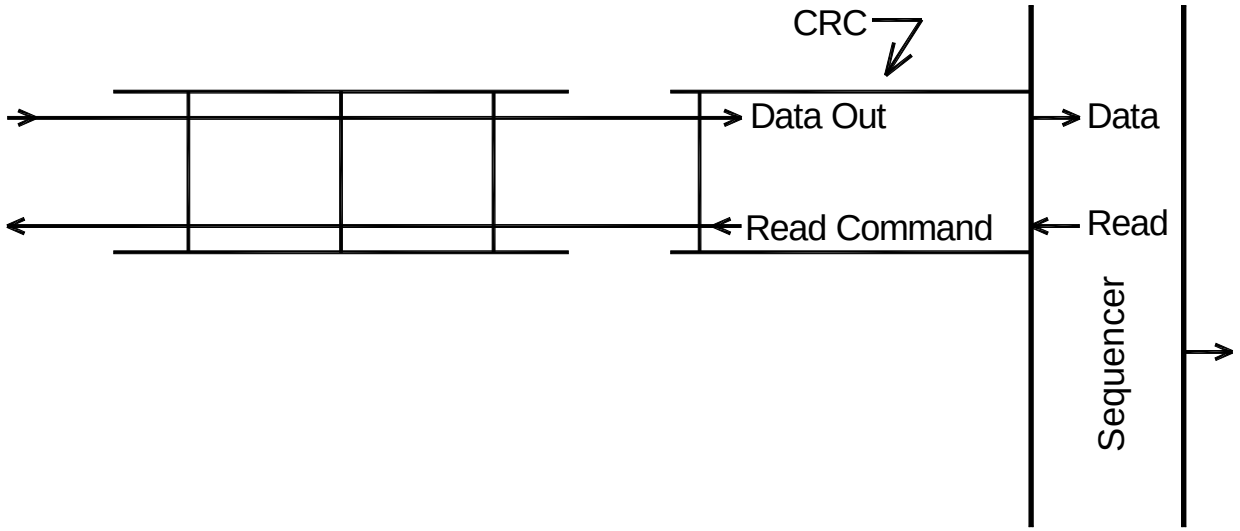
- As a local digital memory to store the time stamp, F/F's are used. To express 3000 bunches, 12 bits are needed and 13th and 14th bits are for checking the parity. Since average multiple impact probability per pixel is assumed to be 4, 14 (H) x 4 (V) F/F's are needed in this architecture.
- When a particle impacts, a pixel's signal rises above the threshold level and comparator out switches from '1' to '0', enabling the F/F's to latch the time stamp data supplied by the global bunch counter. When the data is latched, the pixel is reset.
- If next particle impacts the same location, comparator out enables next set of F/F's to preserve the previous time stamp data. This is implemented using a counter which increments the row address of the F/F array.
- Time stamp information is read out in the random access mode from the pixels of interest which stored nonzero time stamp data.

Read Out Logic

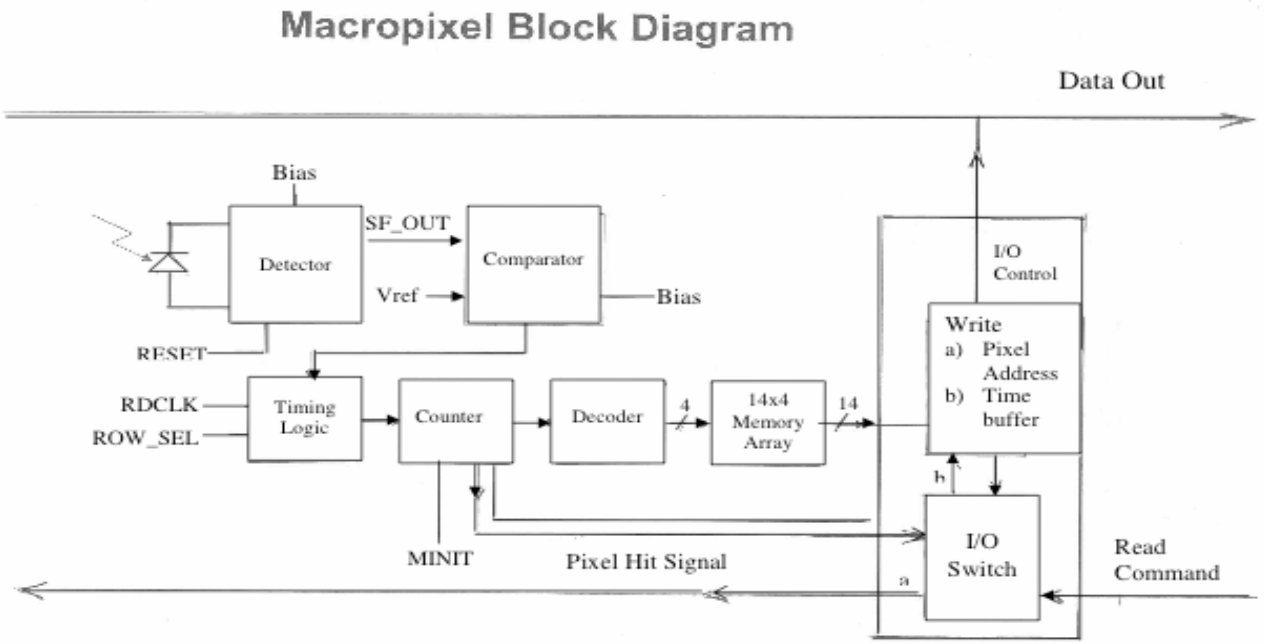
a) CMOS Chip



b) Single Column



Macropixel Block Diagram



I/O Control Operation

a) Pixel not hit – I/O Switch in position a – Read command passed on to next pixel

b) Pixel hit – I/O switch in position b – Read out Pixel
– then turn I/O Switch to position a

Readout Procedure and Speed

- Expected hit rates:
  - Consider chips 22 mm x 125 mm = 2750 mm^2
  - Total no. of 10 μ x 10 μ pixels = 27.5×10^6 pixels/chip
  - Total hits .03 x 2820 x 2750 = 2×10^5 hits/chip
- Number of bits to read out one hit pixel

  X info (up to 2200) – 12 bits + parity = 13 bits
  Y info (up to 12500) – 14 bits + parity = 15 bits
  Time (up to 3000) -12 bits + parity = 13 bits
  41 bits total
- 2×10^5 hits/chip x 41 bits/hit/50 MHertz = 164 milliseconds
- We can divide each chip into 10 or 20 paralell readout streams to accommodate higher background rates.

Read Noise

- Minimum ionizing particle leaves ~80e^- /micron in expitaxial layer

  10 μ thick epi x 80e^-/μ = 800 e^-

- Would like signal to noise of ~ 10 to 20

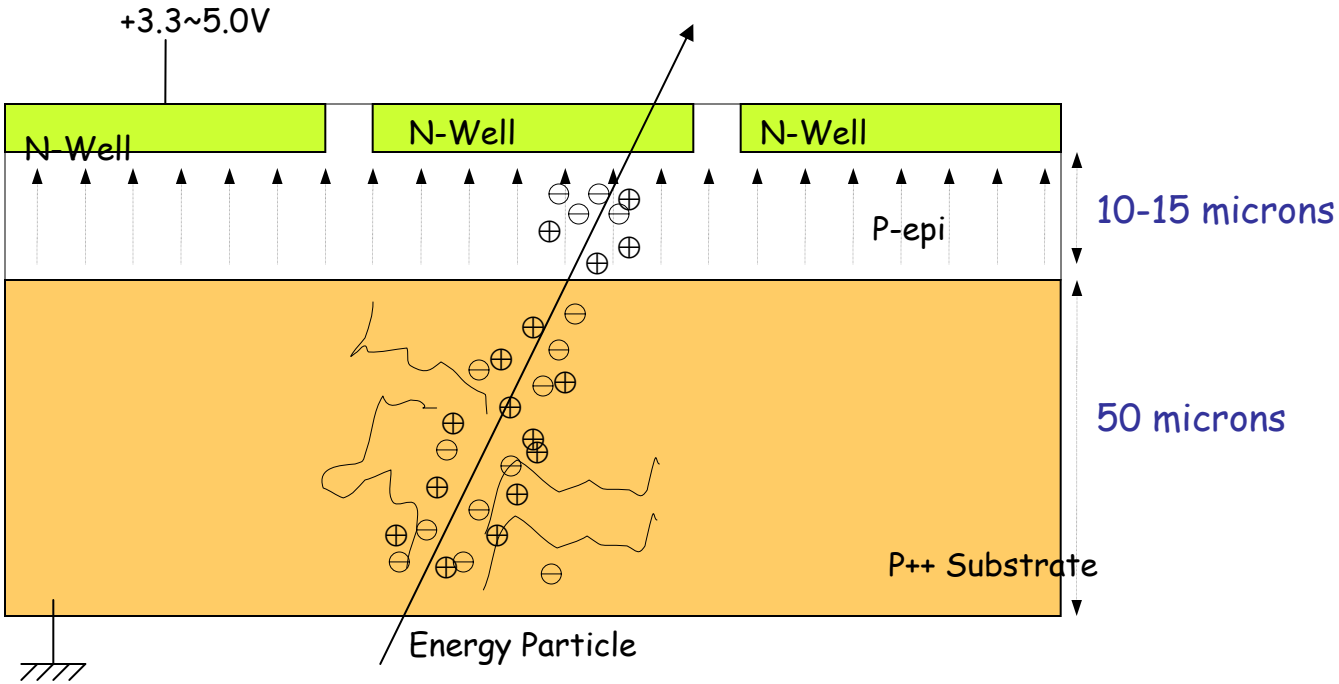
Can keep read noise below 40 e^- or so

This consideration determines the thickness of the epitaxial layer.

Charge Spreading

- It is important to keep charge spreading to much smaller than the pixel size so that we can give up on the analog information.
- How small can we keep the charge spreading
  - Thickness of expitaxial layer – 10 to 15 μ
  - Fully deplete expitaxial layer – need high resistivity, 1000-2000 ohmcm
  - -- Can keep charge spreading to a few microns

CMOS Pixel Vertical Cross Section



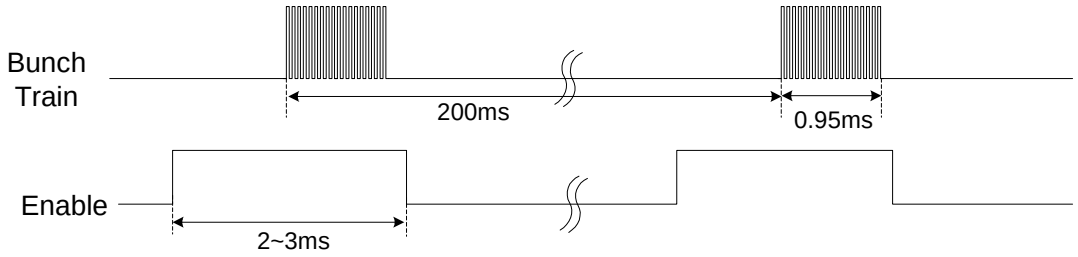
- Entire P-epi region is assumed to be depleted and p++ substrate region is not depleted.
- Electron is the minority carrier in p++ substrate and p-epi.
- Electrons generated in the p++ substrate will diffuse around but can not travel far because they recombine quickly with holes that are abundant in the p++ sub.
- Electrons generated in the epi-region are forced move toward N-well diode region by the electric field and do not have the chances of recombination.
- In conclusion, spread is minimum even if the CMOS wafer is not thinned. Epi-thickness and electric field are the factors to determine the lateral spread function.

Power Dissipation Analysis

	Component	Optimized Power Dissipation	Before Optimization
Analog	Detector	9.9uW	11.7uW
	Comparator	27.0uW	35.1uW
	Sub_total	36.9uW	46.8uW
Digital	Timing Logic	0.05uW	
	Counter/Decoder	0.07uW	
	Mem. Array	~ 0uW	
	IO Interface	0.01uW	
	Sub_total	0.13uW	
	Total	37.03uW	

- **Additional 67- to 100-fold reduction expected by power cycling analog components (0.37 – 0.55 uW per pixel)**

Power Reduction Method



* Activate the Detector and the Comparator during the Bunch Train (~1msec) and deactivate during the Readout time(200 msec)
* Power reduction Ratio 1/67 to 1/100
* 0.37 to 0.55 Watts per 2cmx12.5cm chip

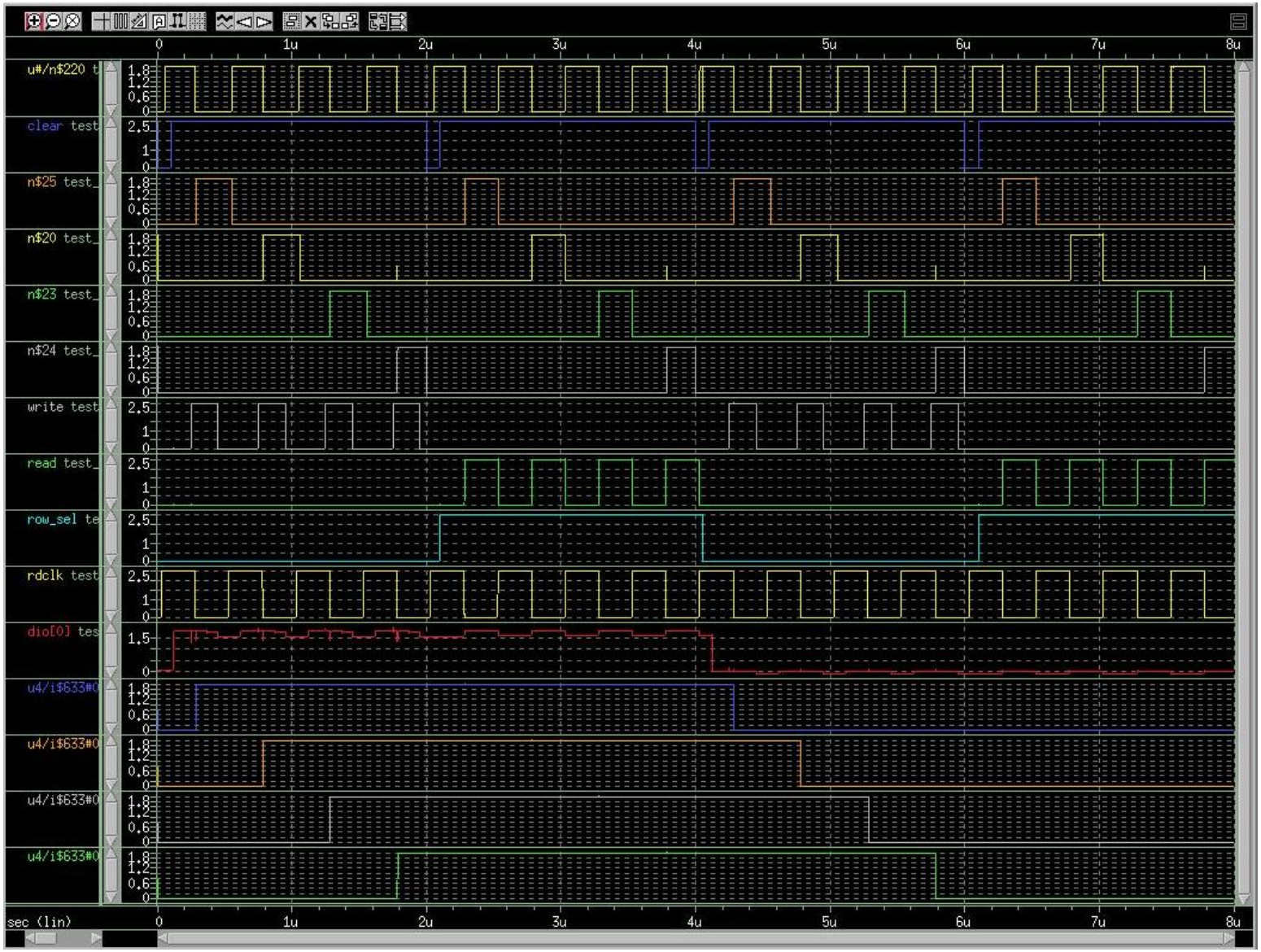
Other Considerations

- Dark Current
  - Will reset array after each bunch crossing so dark current should not be a problem during 337 nanosec
- Operating Temperature
  - Sarnoff expects modest cooling (<0°C adequate)
- Device Thickness
  - Thinning below 50 um looks feasible ~
- B Field – Lorentz angle is an issue

Present Progress and Plan

- Completed macropixel design
  - 645 transistors per pixel!
  - Spice simulation verifies design
  - TSMC 0.18 um -> 40-50 um pixel at present
- Next phase under consideration
  - Complete design of prototype chip
  - Deliverable –tape out for foundry
- Future
  - Fab first prototype with 50 um pixels
  - Then, proceed to 10 um design

Spice Model Verification of Design

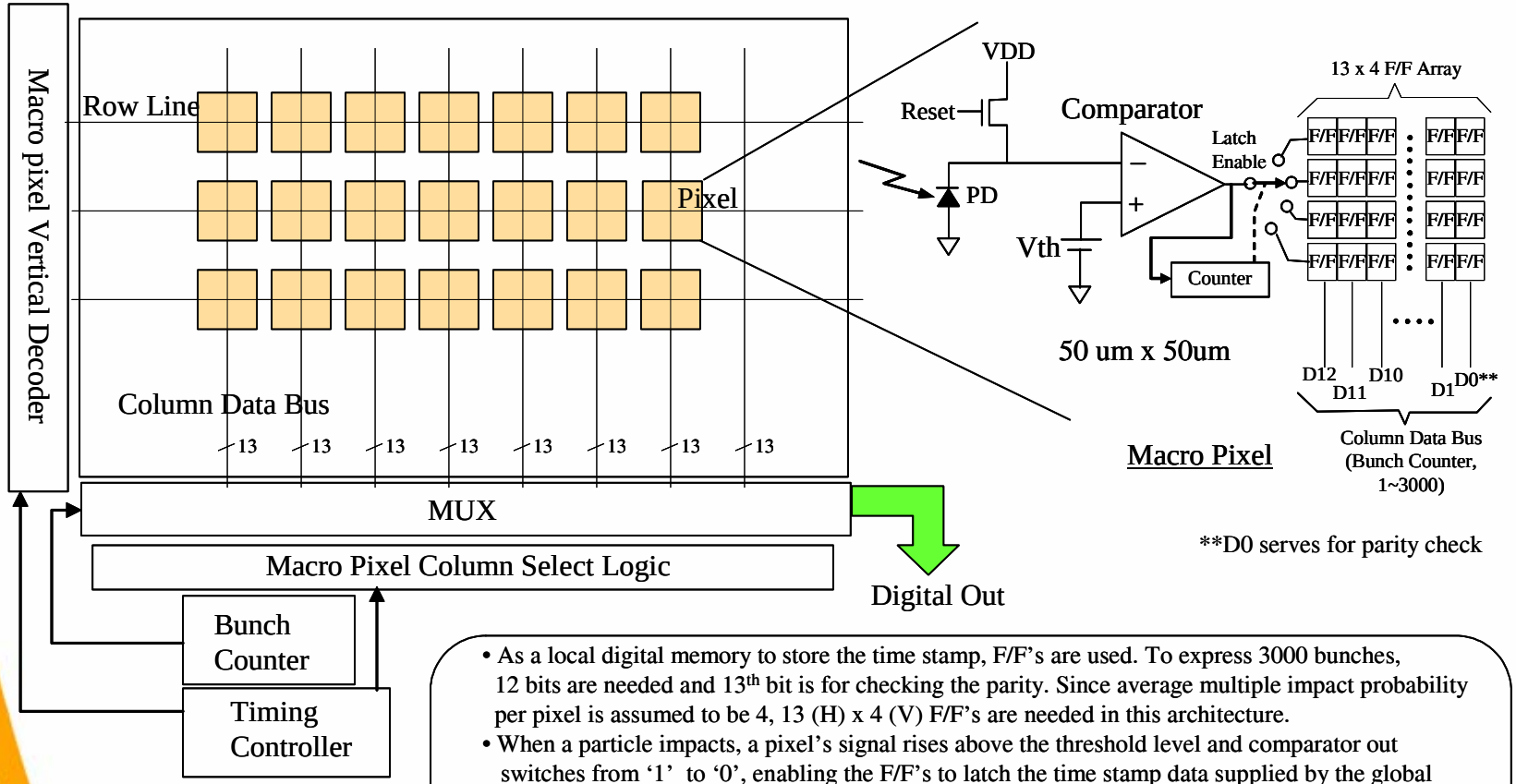


Issues and concerns for future R&D

- Can power consumption be reduced further? How will it scale as we go to 10 micron pixels?
- Readnoise will have to be evaluated as more detailed design progresses.
- How will voltages to fully deplete epi-layer scale to the 45 nm technology?
- Many other issues as detailed design procedes and moves toward 10 micron pixels

Extra Slides

Macro Pixel Array Architecture



**D0 serves for parity check

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SARNOFF Corporation

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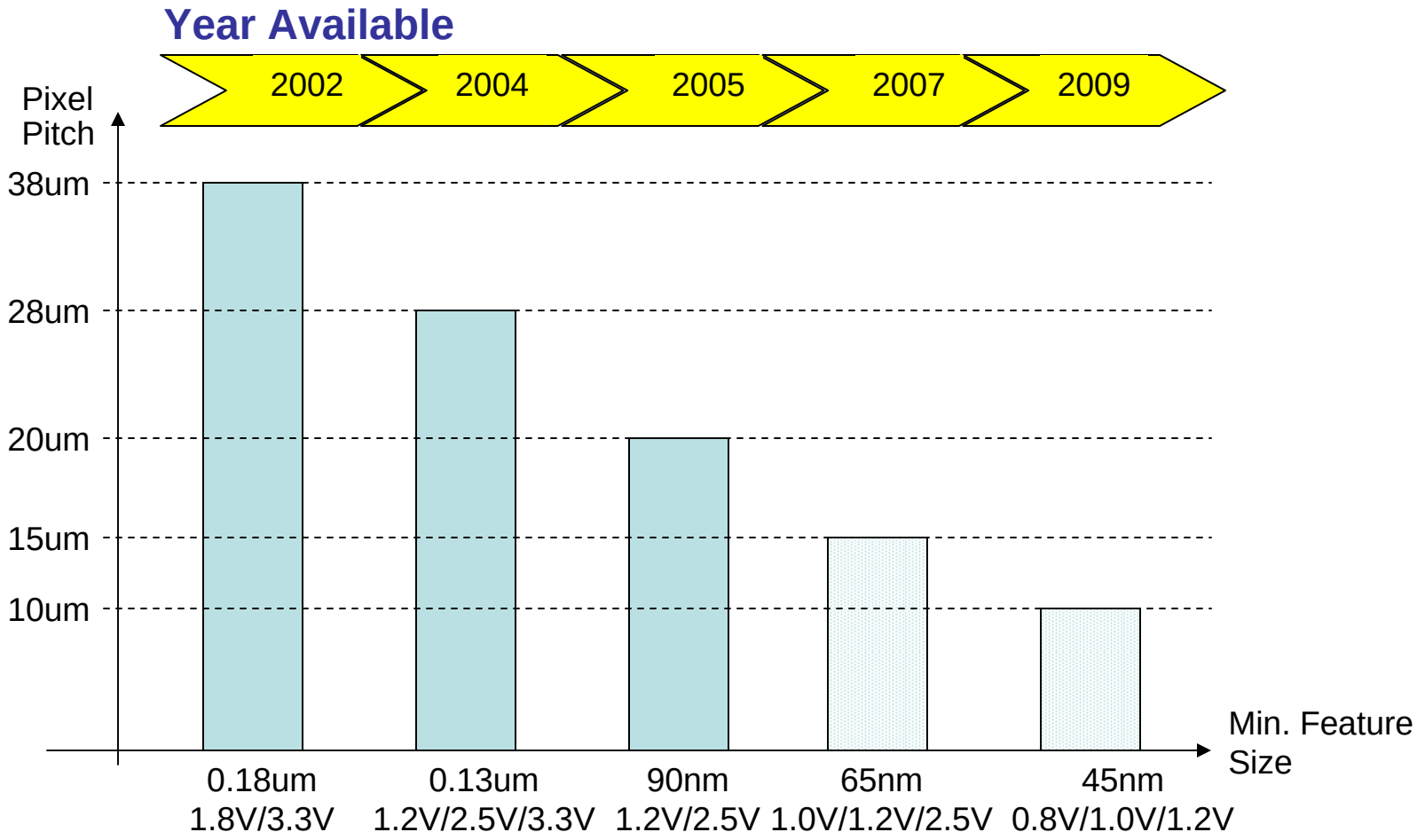

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