CMOS MAPS with fully integrated, hybrid-pixel-like analog front-end electronics

L. Ratti[a,c], C. Andreoli[a,c], M. Manghisoni[b,c], E. Pozzati[a,c], V. Re[b,c], V. Speziali[a,c], G. Traversi[b,c], S. Bettarini[d], G. Calderini[d] R. Cenci[d], F. Forti[d], M. Giorgi[d], F. Morsani[d], N. Neri[d], E. Paoloni[d] , G. Rizzo[d]

[a]Università degli Studi di Pavia

[b]Università degli Studi di Bergamo

[c]INFN Pavia

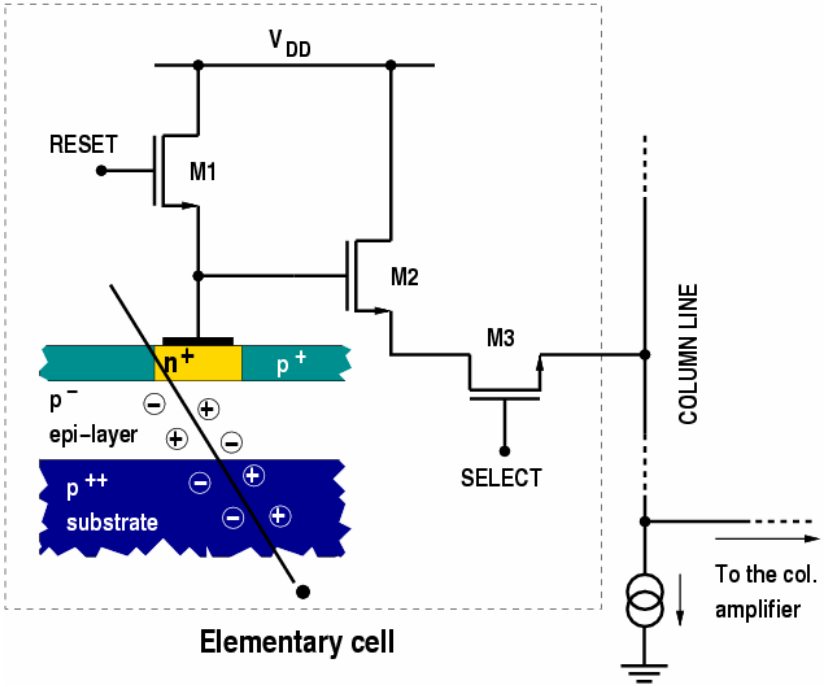
[d]INFN Pisa and Università degli Studi di Pisa

for Particle, Astroparticle and Synchrotron Radiation Experiments

Outline

- CMOS MAPS fundamentals
- Deep N-well (DNW) MAPS in CMOS technology
- The apsel0 prototype: characterization results
  - Front-end electronics characterization
  - Radiation source test results
- The apsel1 prototype: preliminary characterization results
- Towards applications to experiments in future colliders

Conventional CMOS MAPS



P-type, high resistivity, epitaxial layer acts as a potential well for electrons (Feasibility in non epitaxial CMOS processes has been demonstrated by Dulinski et al., *IEEE TNS* **51** (2004) 1613)

Electrons diffuse until they reach the n-well/epi-layer junction

Charge-to-voltage conversion is provided by sensor capacitance

Simple, mostly 3T, in-pixel readout configuration (no PMOS allowed) (Examples of advanced functions integrated at the pixel level are available in the literature: G. Deptuch et al., NIM A512 (2003) 299)

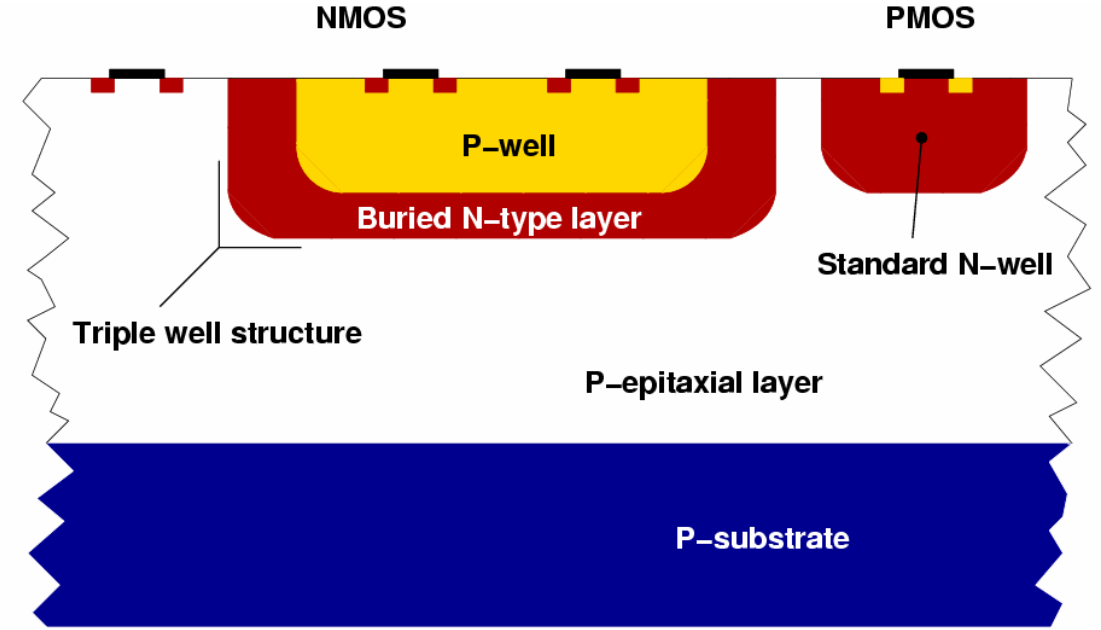
- Front-end integrated on the sensor substrate → compact, flexible system on chip
- Thin sensitive volume (epitaxial layer, ~10 μm) → reduced multiple scattering
- Deep sub-μm CMOS technologies → low power, radiation tolerance, fast readout

→ fast turn-over → continuous technology watch

Why hybrid-pixel-like MAPS

- Modern VLSI CMOS processes (130 nm and below) could be exploited to increase the functionality in the elementary cell → sparsified readout of the pixel matrix.
- Data sparsification could be an important asset at future particle physics experiments (ILC, Super B-Factory) where detectors will have to manage a large data flow
- A readout architecture with data sparsification will be a new feature which could give some advantages with respect to existing MAPS implementations → flexibility in dealing with possible luminosity changes during the experiment lifespan
- An ambitious goal is to design a monolithic pixel sensor with similar readout functionalities as in hybrid pixels (e.g., FPIX2)

Triple-well CMOS processes



- In triple-well CMOS processes a deep N-well is used to isolate N-channel MOSFETs from digital signals coupling through the substrate
- NMOSFETs can be integrated both in the epitaxial layer or in the nested P-well; P-channel MOSFETs are integrated in standard N-wells

DNW-MAPS concept

- Deep N-well (DNW) is used to collect the charge released in the substrate

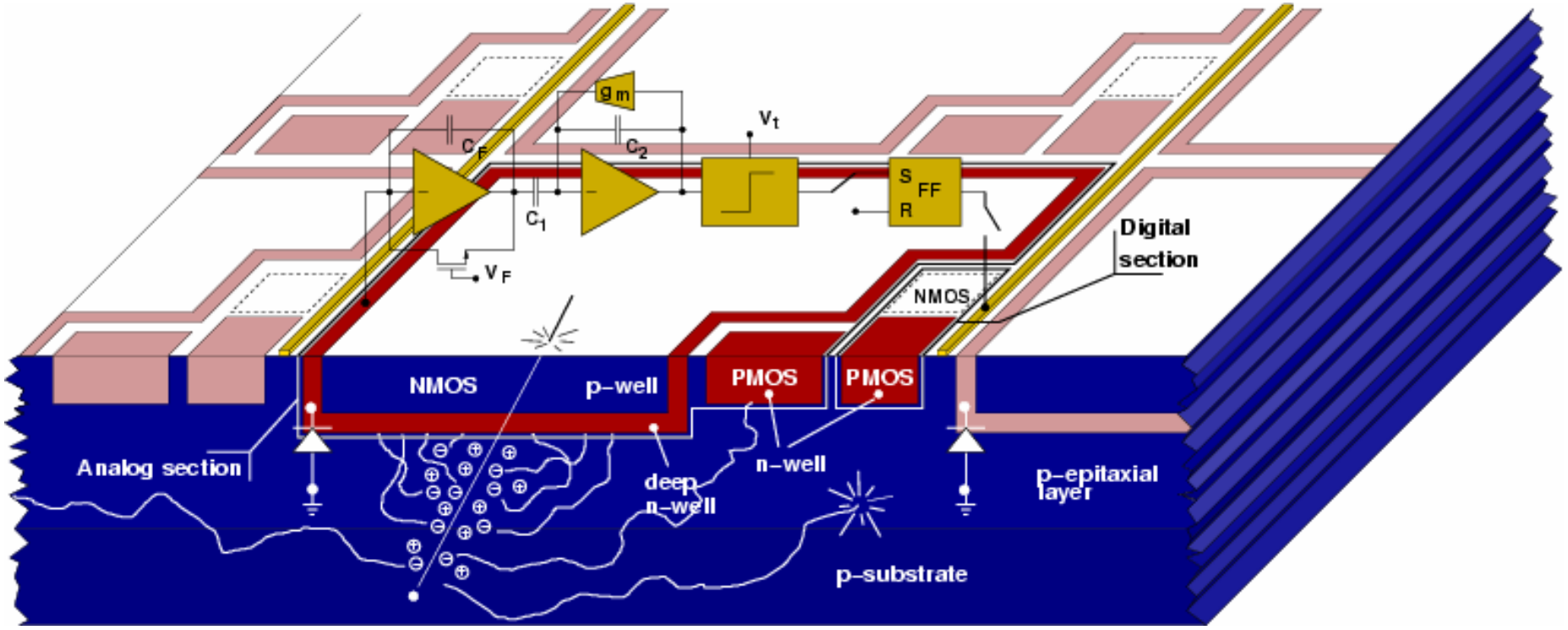
  Use of the deep N-well was proposed by Turchetta et al. (*2004 IEEE NSS Conference Record*, vol. 2, pp. 1222-1226) to address radiation hardness issues

- A readout channel for capacitive detectors is used for Q-V conversion → gain decoupled from electrode capacitance, no correlated double sampling

- VLSI deep submicron CMOS process → high functional density at the elementary cell level

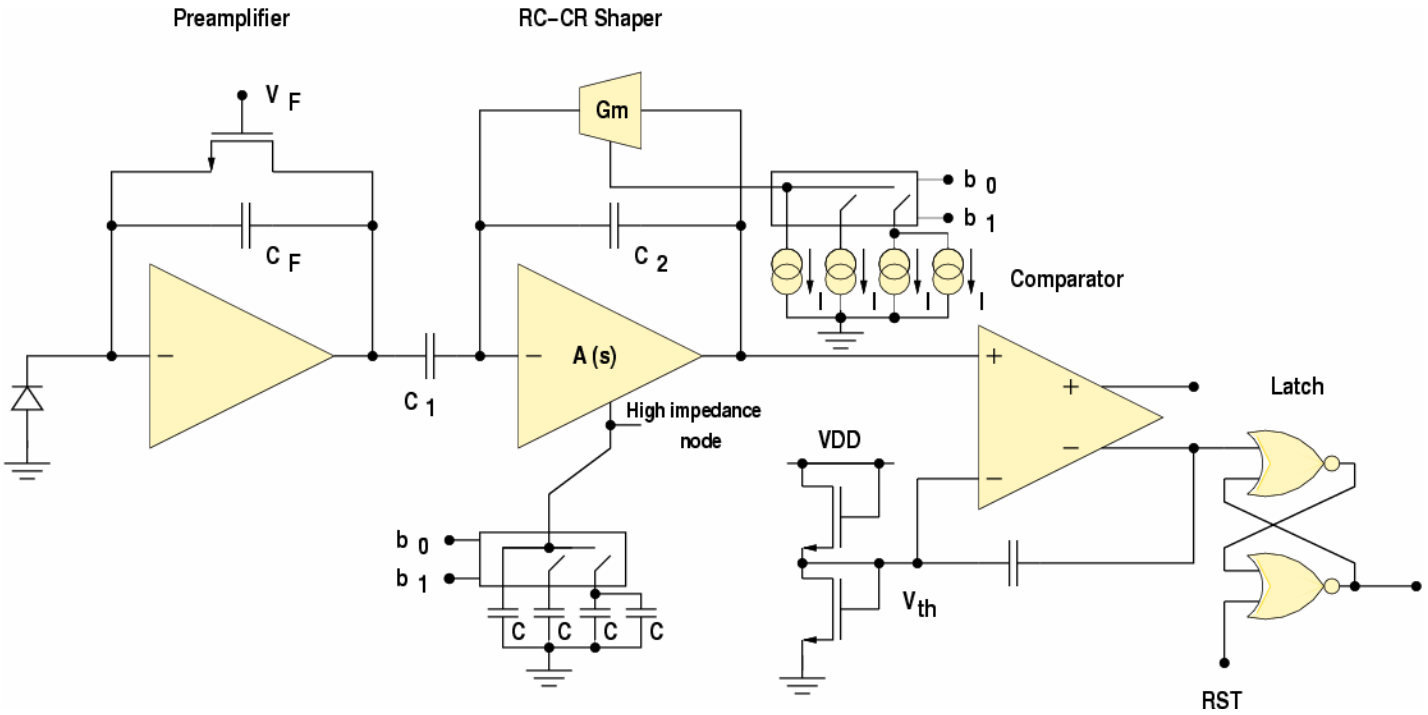
- NMOS devices of the analog section are built in the deep N-well → area covered by the electrode can be reused for the front-end electronics

DNW-MAPS concept



- Bias to the DNW collecting electrode is provided by the preamplifier input
- The DNW takes up a large fraction of the cell → PMOS devices can be safely included in the design

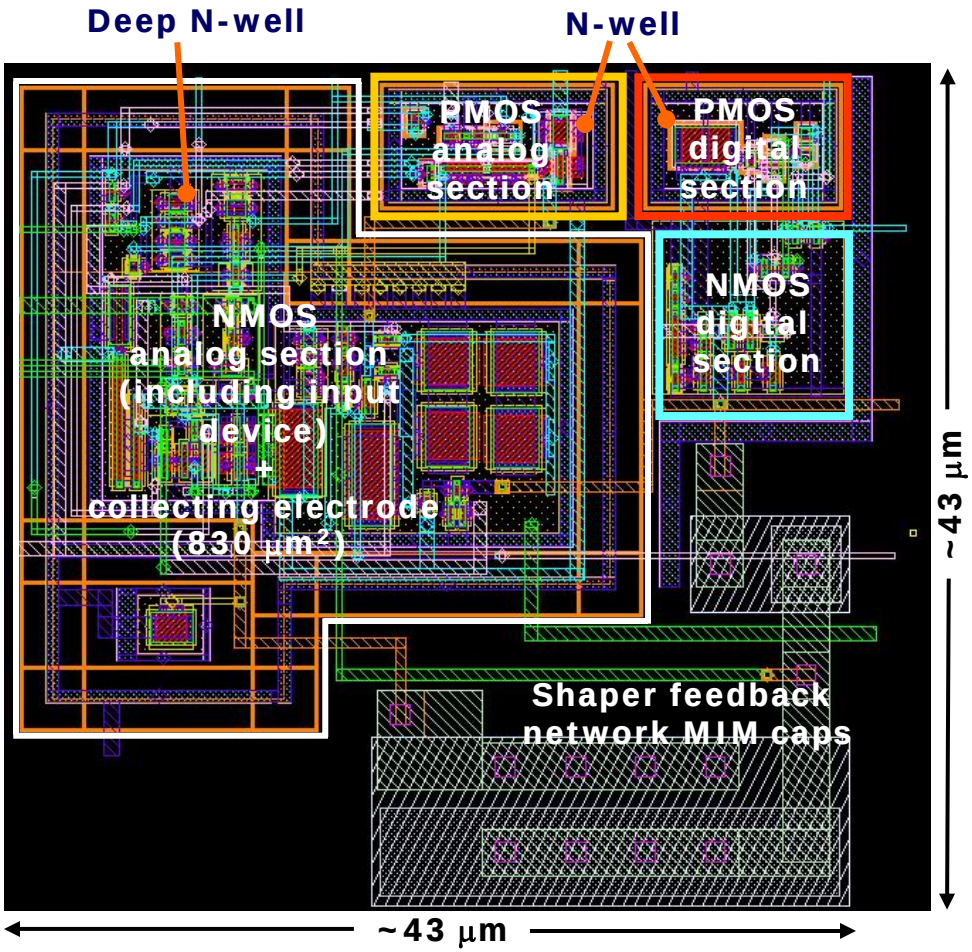
Pixel level processor



- High sensitivity charge preamplifier with continuous reset
- RC-CR shaper with programmable peaking time (0.5, 1 and 2 μs)
- A threshold discriminator is used to drive a NOR latch featuring an external reset

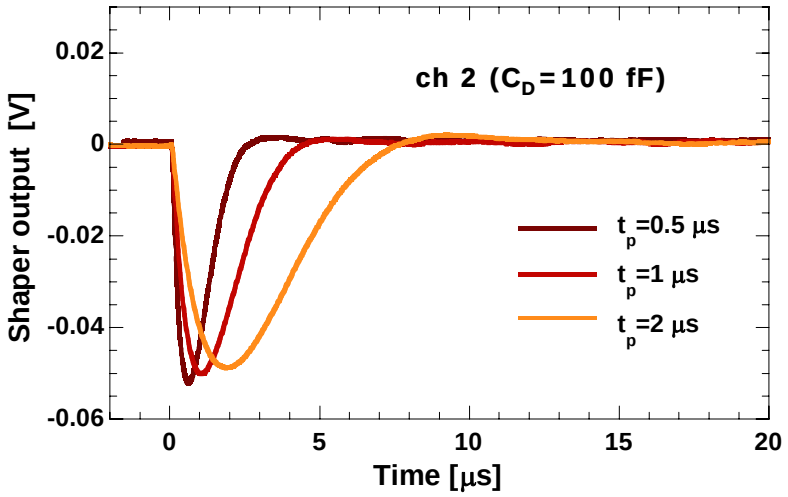
The apsel0 prototype

- 130 nm CMOS HCMOS9GP by STMicroelectronics: epitaxial, triple well process (available through CMP, Circuits Multi-Projets)
- Includes 6 single pixel test structures:
  - 3 with calibration input capacitance (tests with external pulser)
    - ✓ **ch 1**: front-end electronics
    - ✓ **ch 2**: front-end electronics with C_D=100 fF
    - ✓ **ch 5**: DNW-MAPS (830 μm² sensor area, **see picture**)
  - 3 with no injection capacitance (tests with laser and radioactive sources)
    - ✓ **ch 3**: DNW-MAPS (1730 μm² sensor area)
    - ✓ **ch 4**: DNW-MAPS (2670 μm² sensor area)
    - ✓ **ch 6**: DNW-MAPS (830 μm² sensor area)
  - 10 μW/ch power consumption

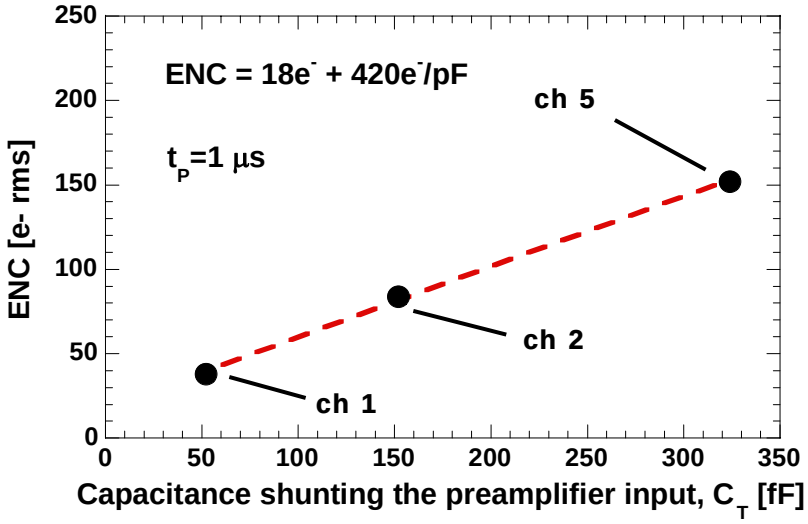


Front-end characterization

Response to a 560 e⁻ pulse



Equivalent noise charge (ENC)



Charge sensitivity [mV/fC]

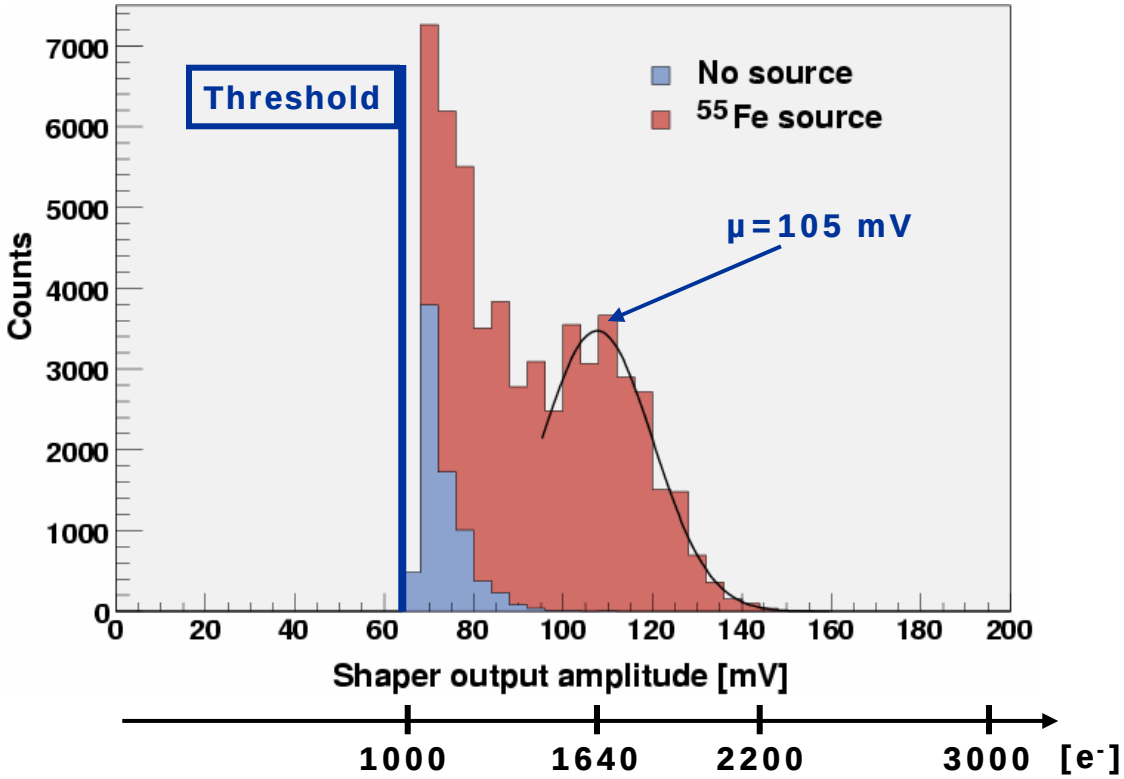
	t_p=0.5 µs	t_p=1 µs	t_p=2 µs
ch 1 (C_D=0)	610	590	530
ch 2 (C_D=100 fF)	580	550	520
ch 5 (C_D=270 fF)	460	450	430

- Change in the charge sensitivity ← small forward gain in the preamplifier, easily reproduced in post layout simulations (PLS)

- ENC ~ C_T, as expected from theory
- No variation with t_p → predominance of 1/f noise contribution (small dimensions of preampli input element, W/L=3/0.35, and relatively long peaking times)
- ENC larger than expected (150 e⁻ for ch 5) ← detector capacitance C_D underestimated: expected value ~100 fF, measured ~270 fF for ch 5)

^{55}Fe source tests

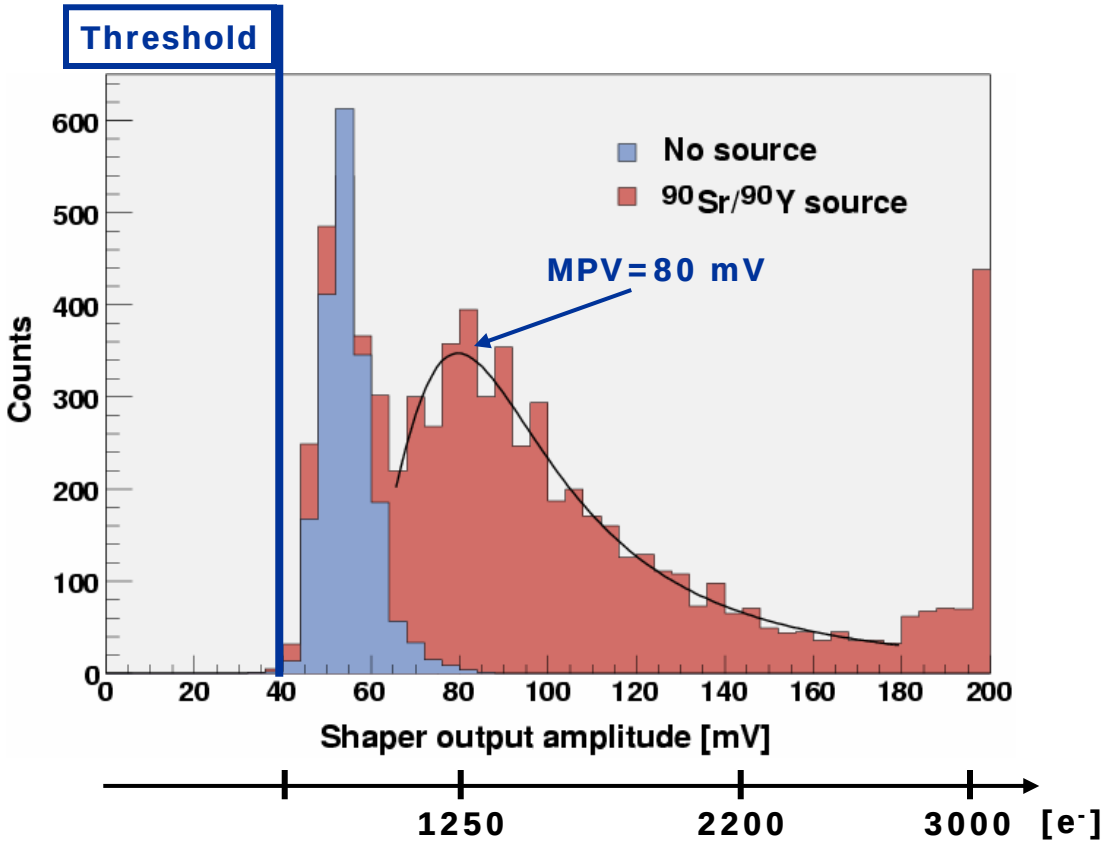
- Soft X-rays from ^{55}Fe to calibrate noise and gain in pixels with no injection capacitance
- Line at 5.9 keV → ~1640 e/h pairs
  - ✓ tests performed at t_p=2 μs on ch 6
  - ✓ peak@105 mV → gain=400 mV/fC (charge entirely collected)
  - ✓ excess of events with respect to noise below 100 mV ← charge only partially collected



- Calibration with ^{55}Fe source in fair agreement with results obtained both with external pulser tests and with PLS (ENC=140 e-, gain=430 mV/fC expected, 125 e- and 400 mV/fC measured from ^{55}Fe calibration)

$^{90}Sr/^{90}Y$ source tests

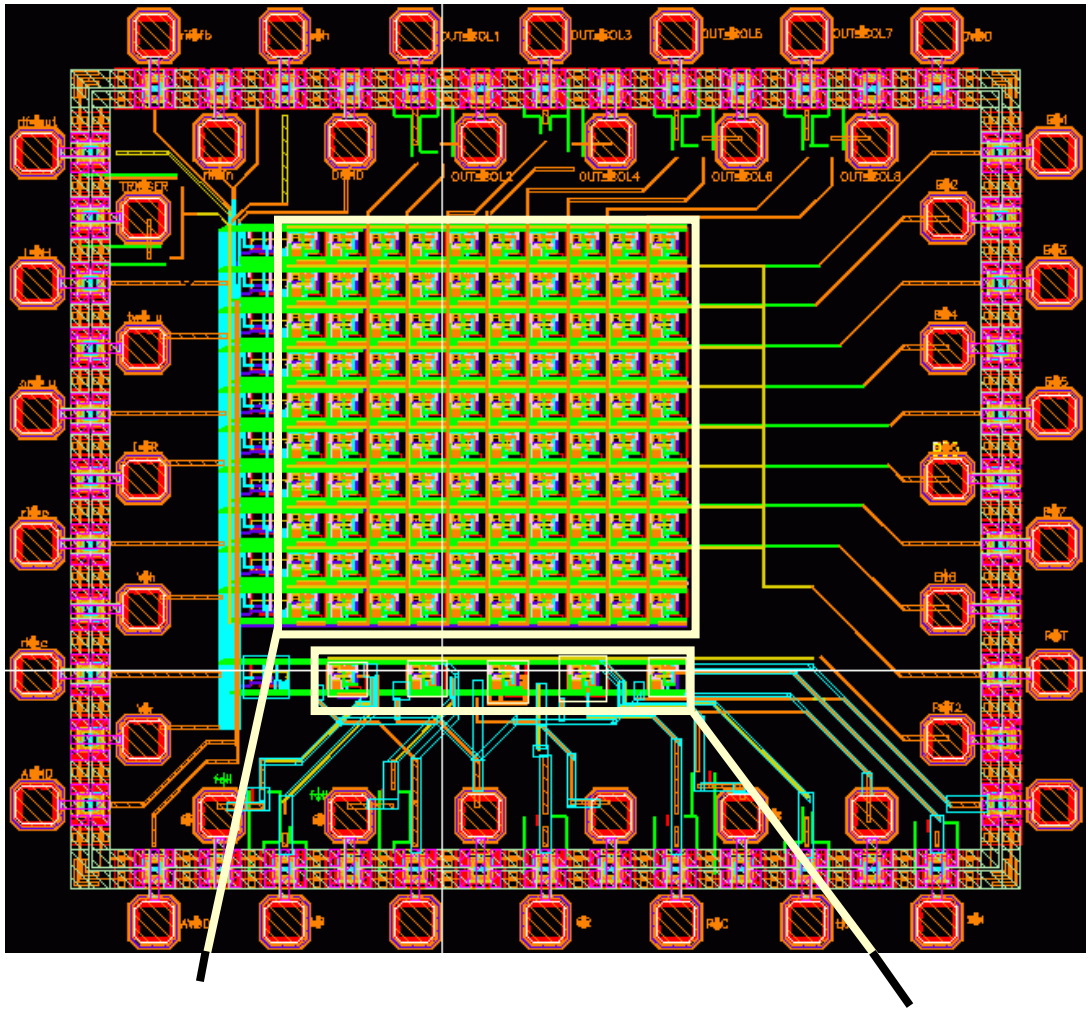
- Landau peak@80 mV
- With the gain measured with ^{55}Fe calibration, M.I.P. most probable energy loss corresponds to ~1250 e^-
- Based on the average pixel noise, S/N=10
- Excess of events towards 200 mV ← saturation due to low energy particles



- Fair agreement with device simulations: ≤ 1500 e^- expected in the case of a thick (>15 μm) epitaxial layer featuring a doping concentration in the order of 10^{15} cm^{-3} (not exactly so in the actual device…)

The apsel1 chip

- Submitted August 2005, delivered January 2006
- Charge preamplifier modified to address gain and noise issues
- The chip includes:
  - 5 single pixel cells (with injection capacitance)
    - ✓ standalone readout channel (ROC)
    - ✓ 4 DNW MAPS with different sensor area (→ different C_D)
  - an 8 by 8 MAPS matrix (50 μm pitch) capable of generating a trigger signal as the wired OR of the latch outputs



8 x 8 matrix + dummies

Single pixel test structures

Preliminary results

In the design of the new front-end circuit version, the gain and noise issues raised by the apsel0 prototype were addressed

- ✓ folded cascode and active load stage implemented in the charge preamplifier
- ✓ input element: W/L=16/0.25, optimized for a detector capacitance of about 320 fF
- ✓ drain current in the input stage: 30 μA

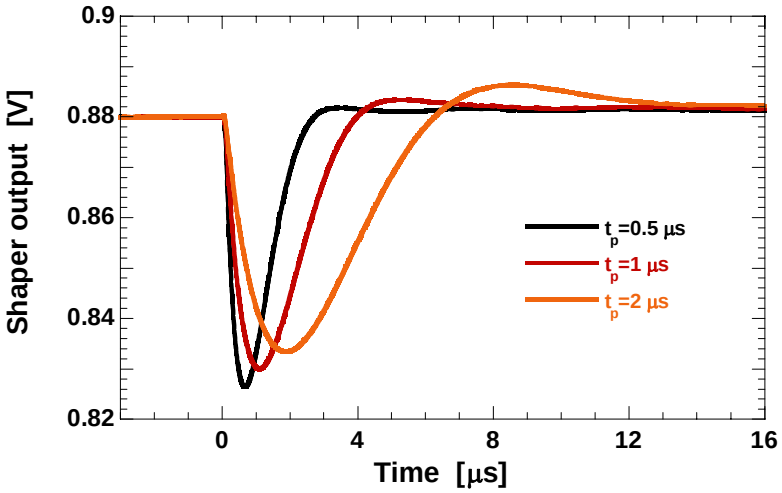
C_D = 320 fF (same as the matrix pixel)

Peaking time [μs]	ENC [e^- rms]	Charge sensitivity [mV/fC]
0.5	41	466
1	39	432
2	39	406

$\frac{dENC}{dC_D}$

Peaking time [μs]	$dENC/dC_D$ [e^-/pf]
0.5	70
1	68
2	68

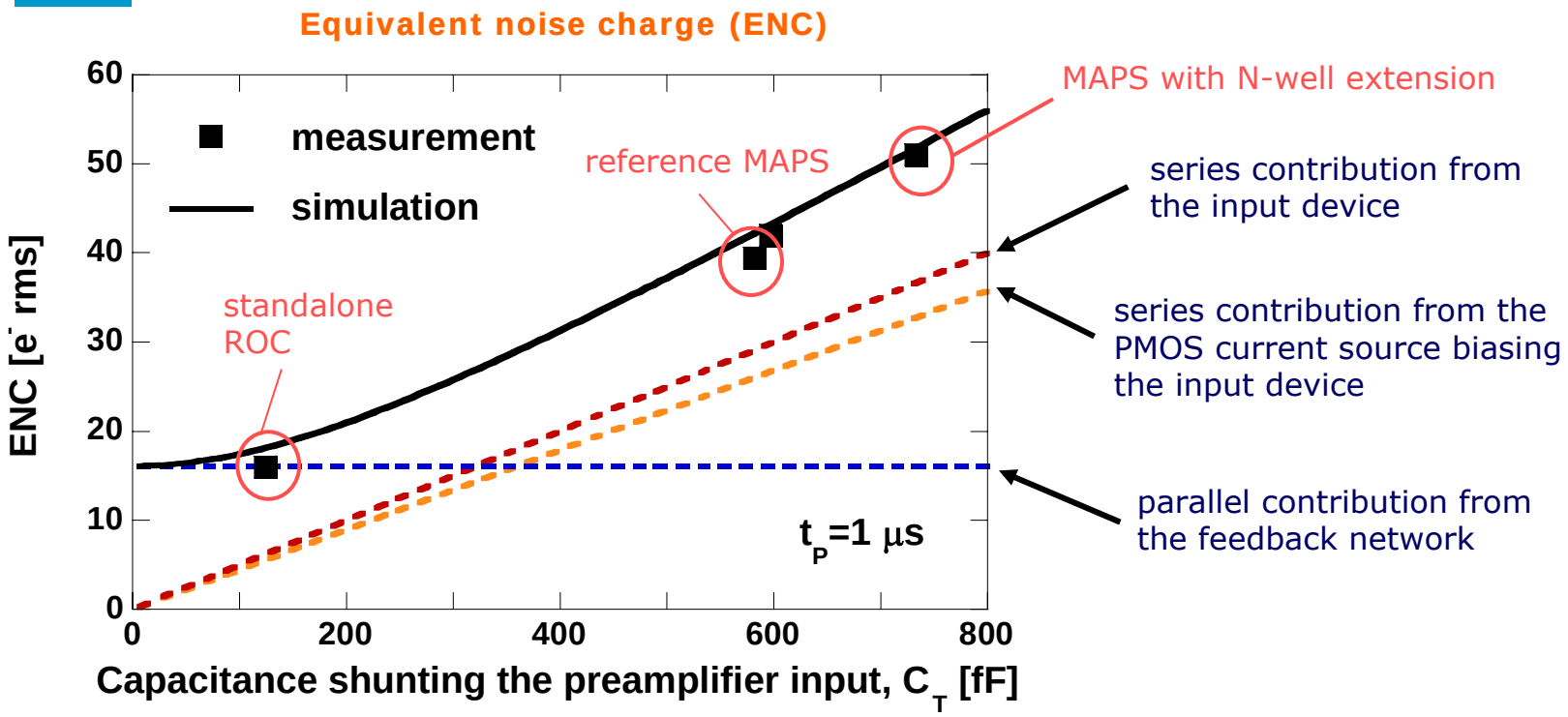
Response to a 750 e^- pulse



Power dissipation (from simulations)

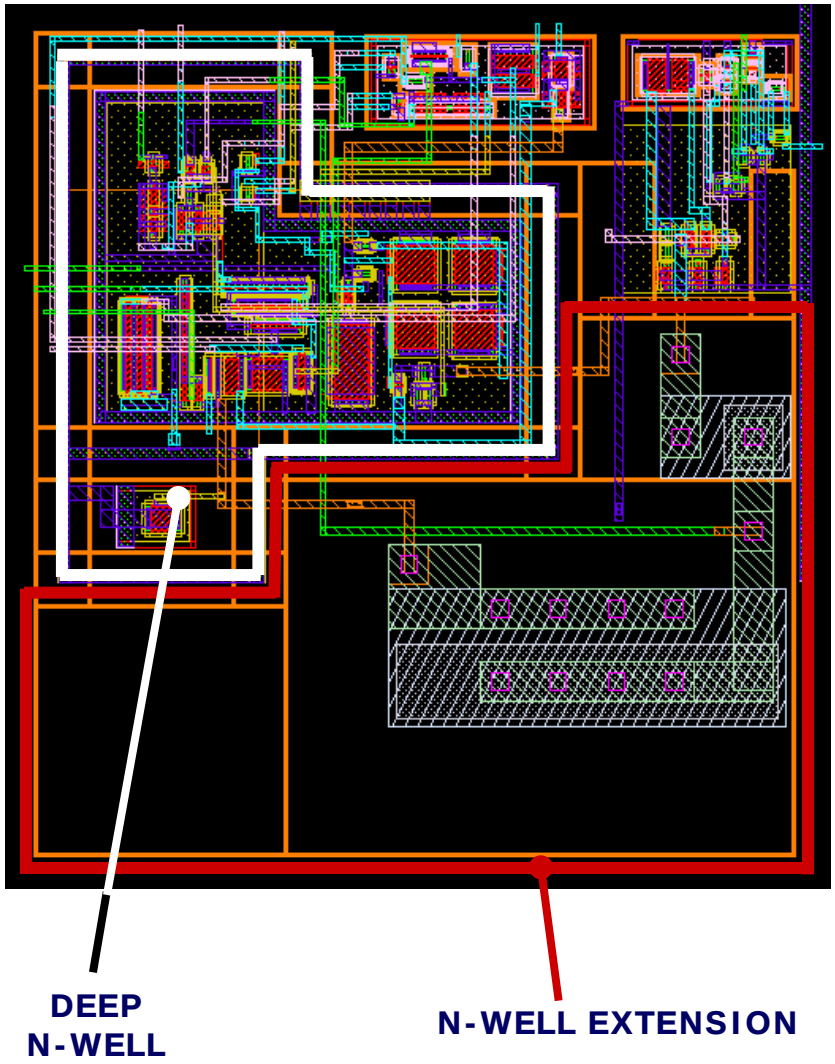
60 μW/channel

Preliminary results

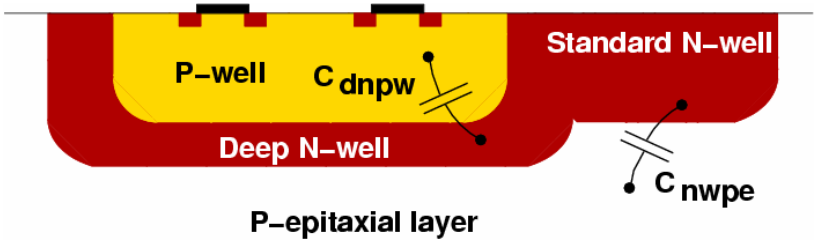


- Noise in the reference MAPS (900 µm^2 in area, the one replicated in the matrix) is ~40 electrons → based on the collected charge figure in ^{90}Sr tests (1250 e$^-$), expected S/N≈30
- ENC in the MAPS with N-well extension (2000 µm^2 collecting electrode area) about 50 e$^-$ → the collector area may be more than doubled with an increase of roughly 25% in ENC

N-well extension



- Standard N-well layer can be used to increase the area of the collecting electrode
- Specific capacitance per unit area of N-well/P-epilayer junction (C_{nwpe}) is about a factor of seven smaller than deep N-well/P-well junction capacitance (C_{dnpw})



- If needed (e.g. to improve charge collection properties), the area of the collecting electrode might be increased with acceptable noise performance degradation

Power cycling

- In future high luminosity colliders, the need to minimize the amount of material in the beam interaction region will put tight constraints on the cooling system → trade-off between power dissipation and operating temperature of the detector
- Power cycling can be used to reduce average dissipated power by switching the chip off when no events are expected
  - Example:
    - ✓ILC bunch structure: ~330 ns spacing, ~3000 bunches, 5Hz pulse
  - Main limitation comes from settling time of voltages and currents in the charge preamplifier (about 20 ms due to the time constant in the feedback network). Settling time is lowered to about 300 μs if the time constant in the feedback network is temporarily reduced
  - In the case of the ILC, power dissipation might be reduced of a factor of more than 100 with respect to continuous operation

Further MAPS miniaturization

- Very high track densities at the next generation colliders will call for highly granular detectors → for binary readout, resolution specifications translate directly into elementary cell size constraints
- Two approaches (not mutually exclusive) presently being pursued:
  - resorting to more scaled technology → improved functional density and, in addition, better noise-power trade-off

    ✓ STMicroelectronics 90 nm, epitaxial process (same substrate and deep N-well properties as in the STM 130 nm technology are expected)

    ✓ activity presently focused on the design of the front-end analog channel (same architecture as in the STM 130 nm design)
  - readout electronics simplification

    ✓ removing the shaper from the processor would halve the number of transistors per cell (from ~60 to ~30)

    ✓ noise degradation should be compensated by sensor area (→ capacitance) reduction

To sum up

- A novel kind of CMOS MAPS (deep N-well MAPS) has been designed and fabricated in a 130 nm CMOS technology
  - deep n-well used as the sensitive electrode
  - standard readout channel for capacitive detectors used to amplify the charge signal
- A first prototype, apsel0, was tested, giving encouraging results and demonstrating that the sensor has the capability of detecting ionizing radiation
- A new chip, apsel1, is presently under test; preliminary results seem to point out that noise and gain issues raised by apsel0 have been correctly addressed
- Other issues, namely power consumption and detector granularity, are being tackled
- Design and submission of a full size MAPS, with hybrid-pixel-like functionalities and implementing data sparsification is planned for the end of this year