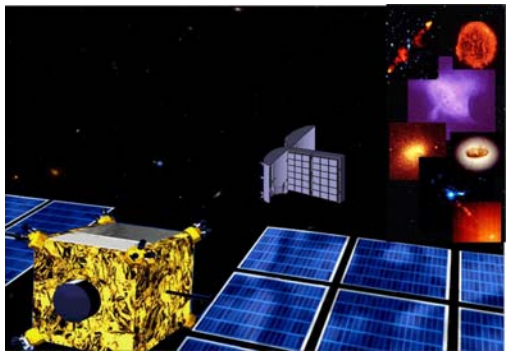
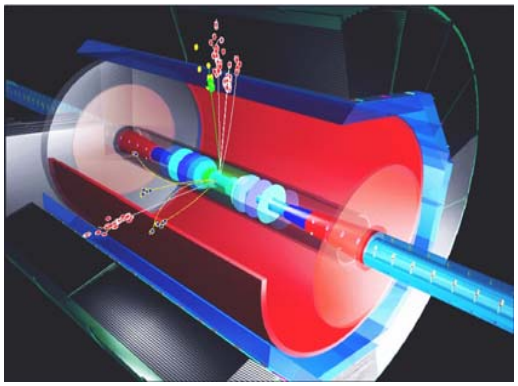
DEPFET Pixel Detectors for Particle and Astrophysics

- DEPFET Principle
- Single Pixel characteritics

- DEPFET prototypes for
  - XEUS
  - ILC Vertex detection

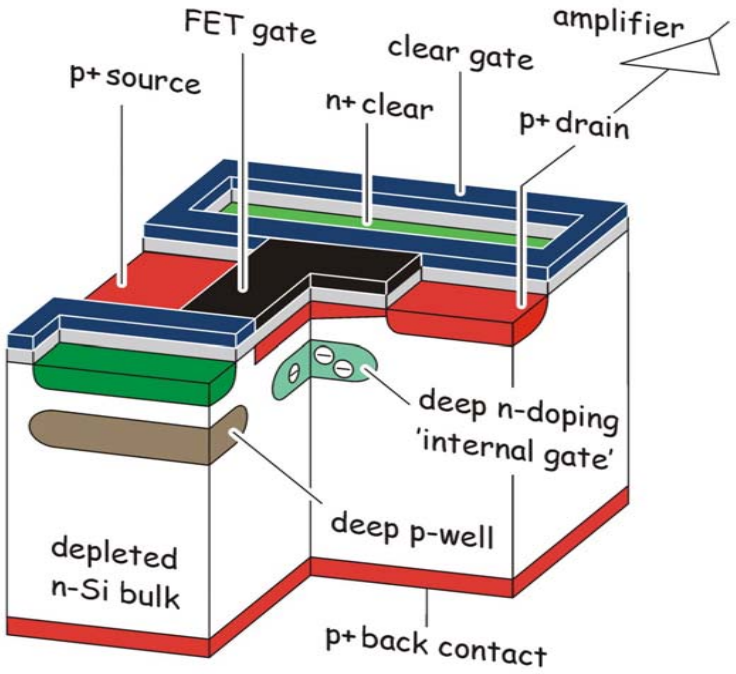


MPI HLL in collaboration with the Universities of Bonn and Mannheim

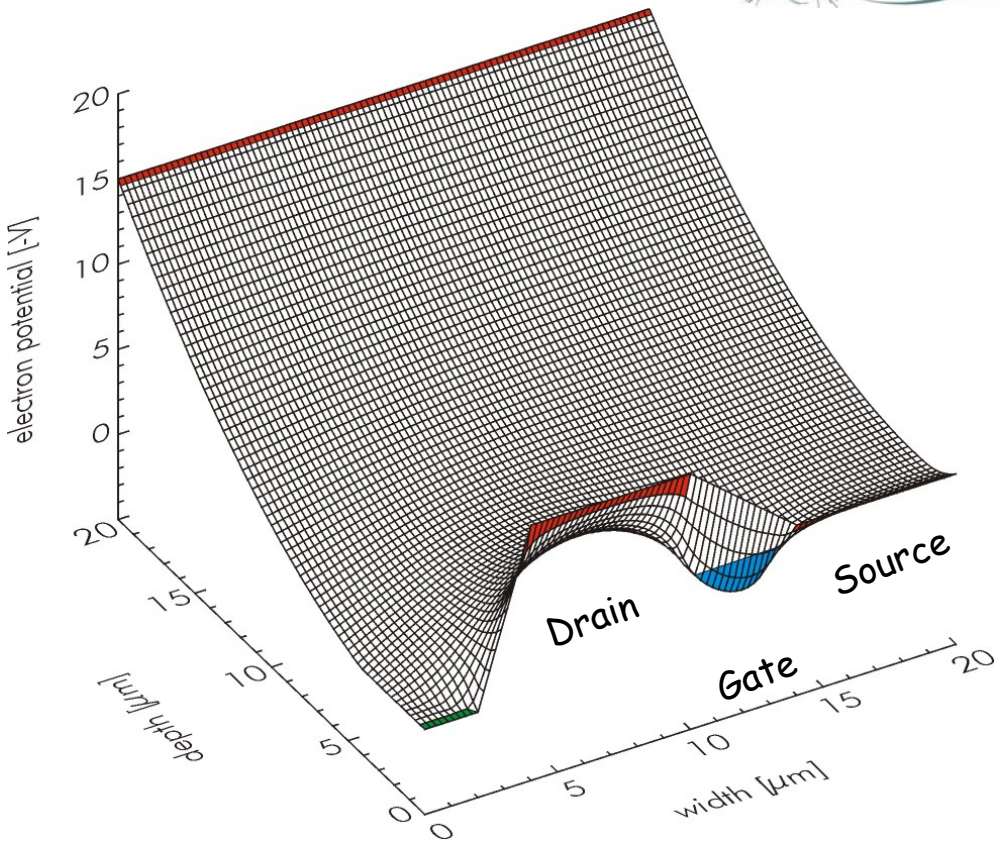


DEPFET Principle

J. Kemmer & G. Lutz, 1987

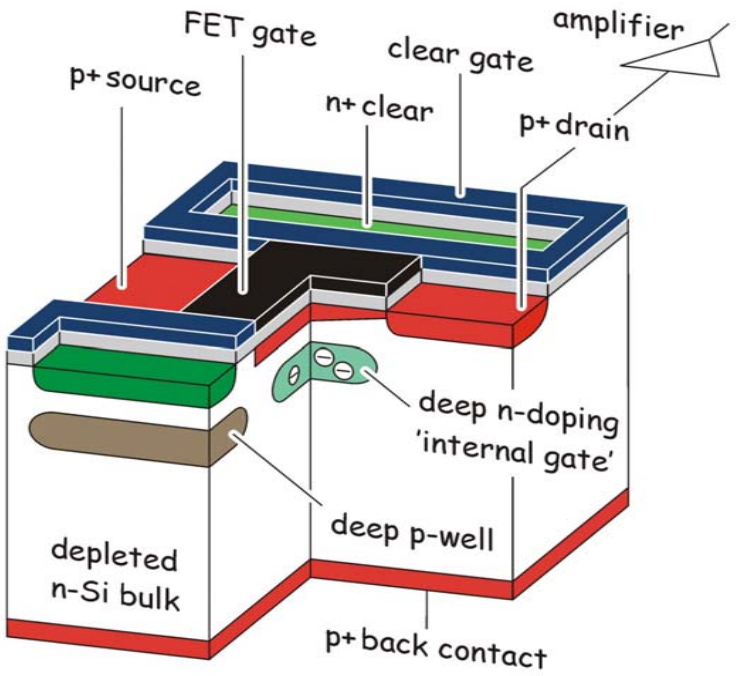


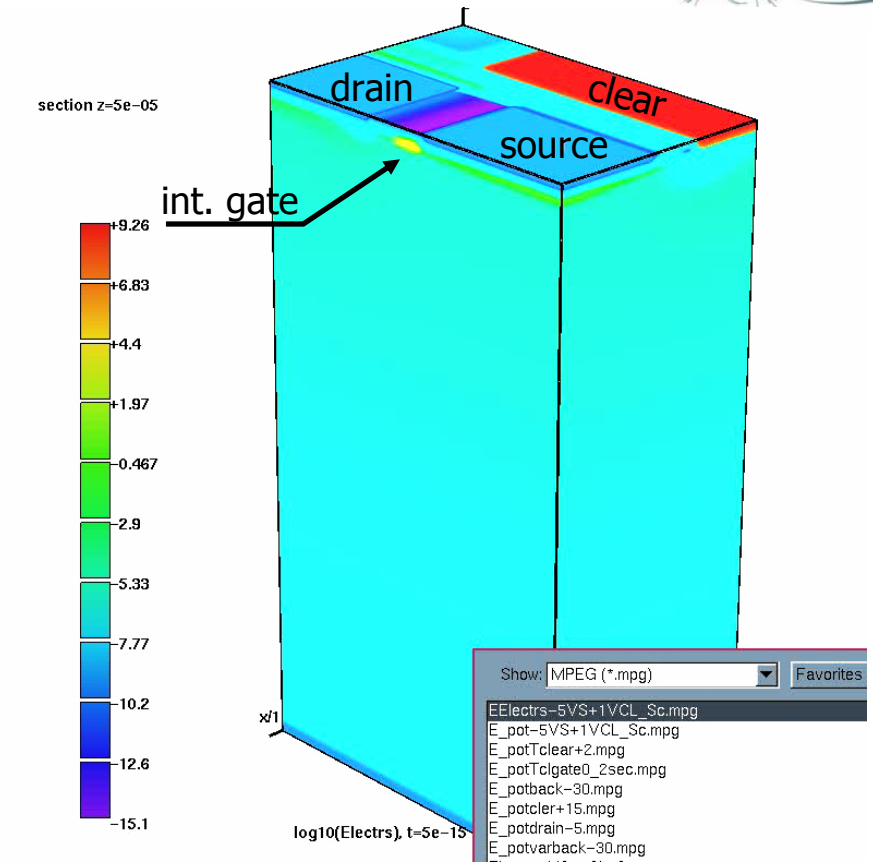
Depleted P-channel FET



- fully depleted sensitive volume
- internal amplification
- Charge collection in "off" state, read out on demand

DEPFET Principle

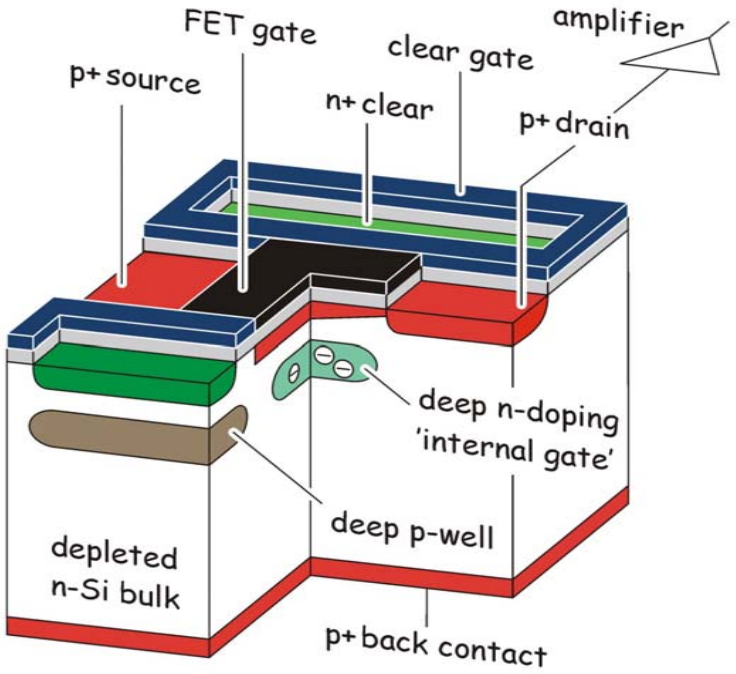


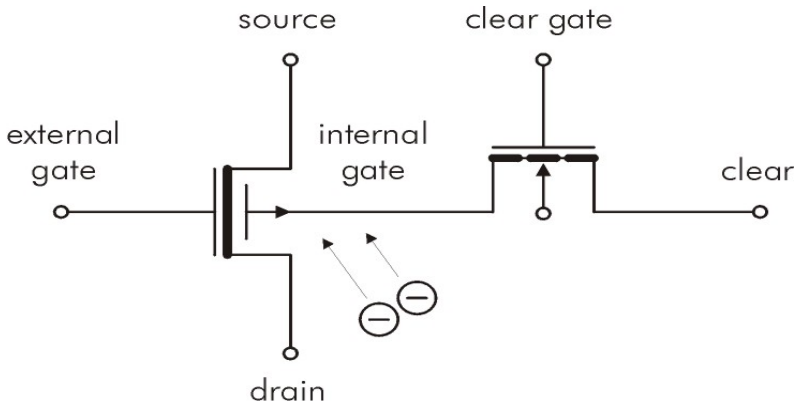


TeSCA 3D Simulation by K.Gärtner, WIAS, Berlin

- fully depleted sensitive volume
- internal amplification
- Charge collection in "off" state, read out on demand

DEPFET Principle

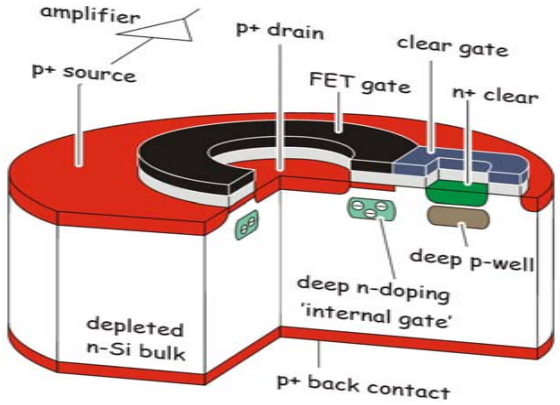




Circuit schematic

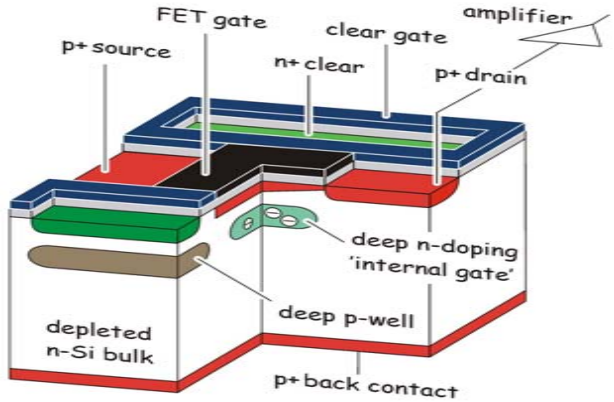
- fully depleted sensitive volume
- internal amplification
- Charge collection in "off" state, read out on demand

Overview: Types and Applications



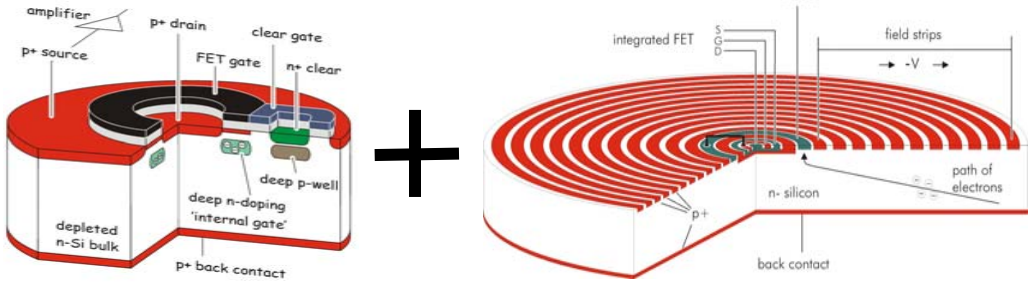
X-ray imaging spectroscopy → XEUS

- pixel size: 100μm
- r/o time per row: 2.5 μs
- Noise: ≈4 el ENC



Particle tracking → vertex detector at ILC

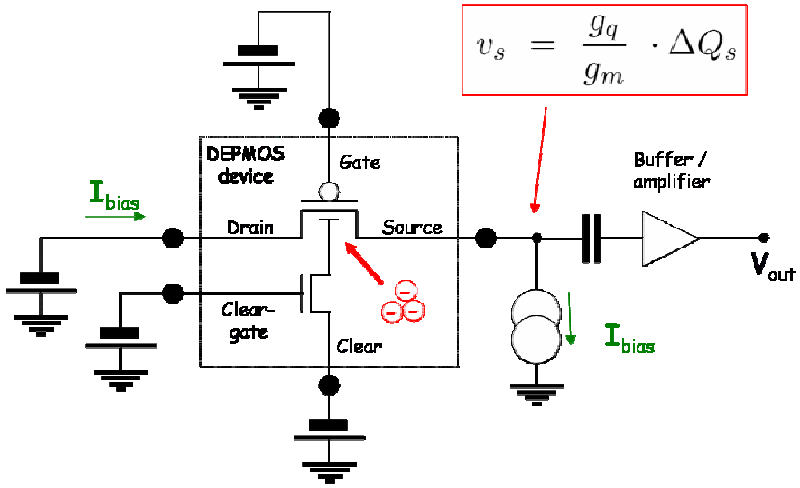
- pixel size: 25μm
- r/o time per row: 20..40ns
- Noise: ≈100 el ENC
- thin detectors: ≈50μm

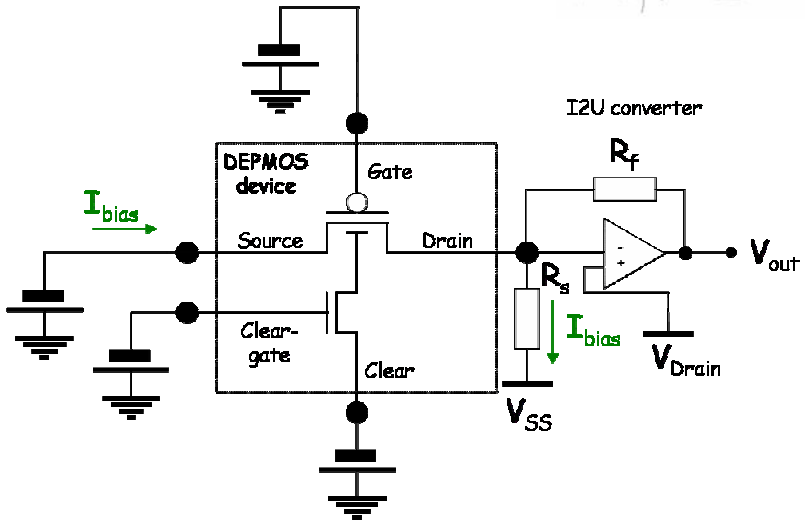


X-ray (imaging) spectroscopy
DEPFET MacroPixel

- pixel size: 100s of μm

Source Follower vs Drain Readout

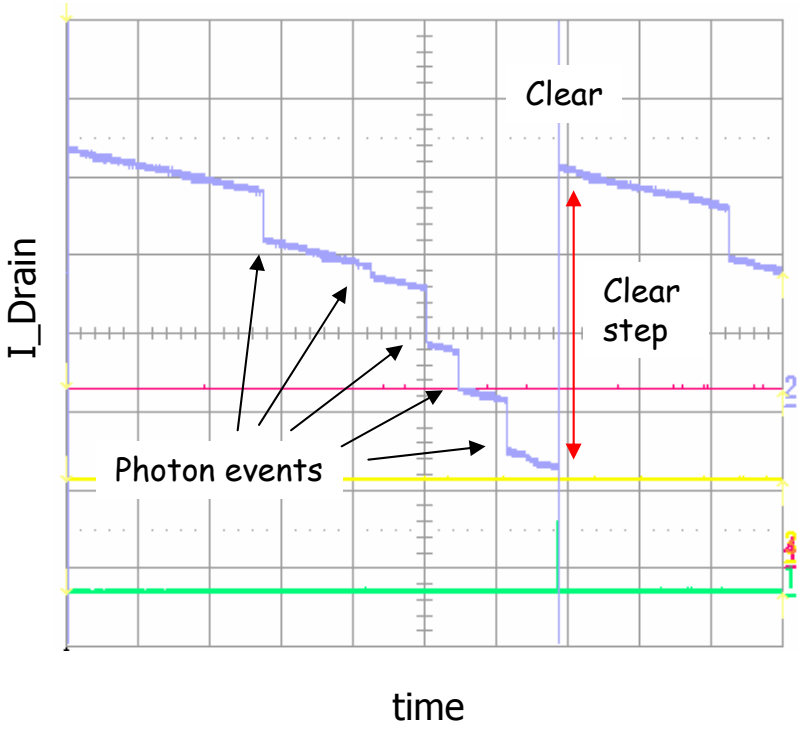




- Constant bias current I_{Bias}
- Change in channel conductivity translates into ΔV_{Source}
- Low noise due to direct voltage amplification
- Speed depends on overall source capacitance (≈µs)

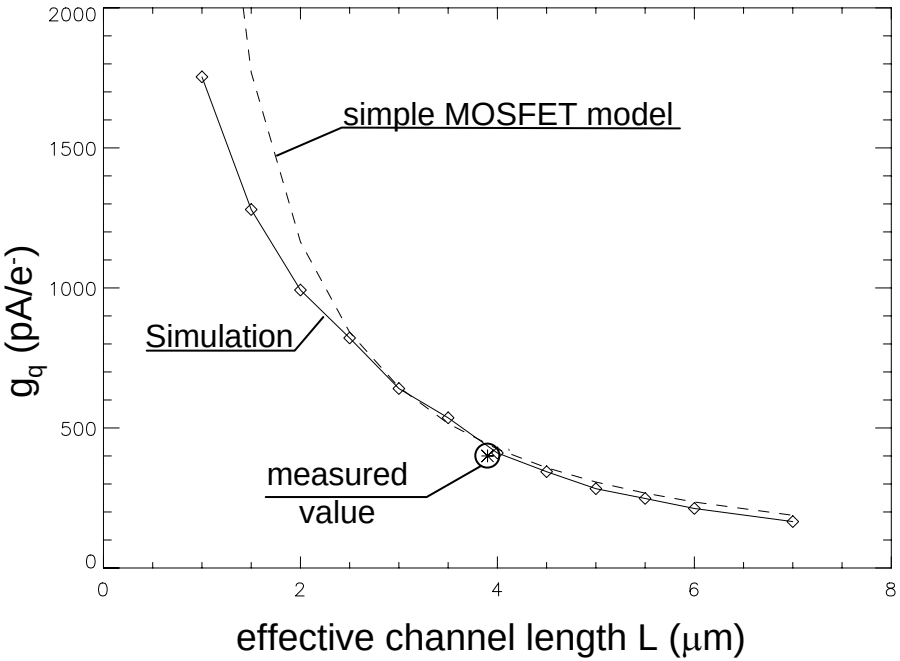
- Drain voltage kept constant
- Change in channel conductivity translates into ΔI_{Drain}
- Control of all bias parameters
- Fast(!) - signal rise time limited by R_{in}, gate settling time... (≈ns)

Internal Amplification g_q



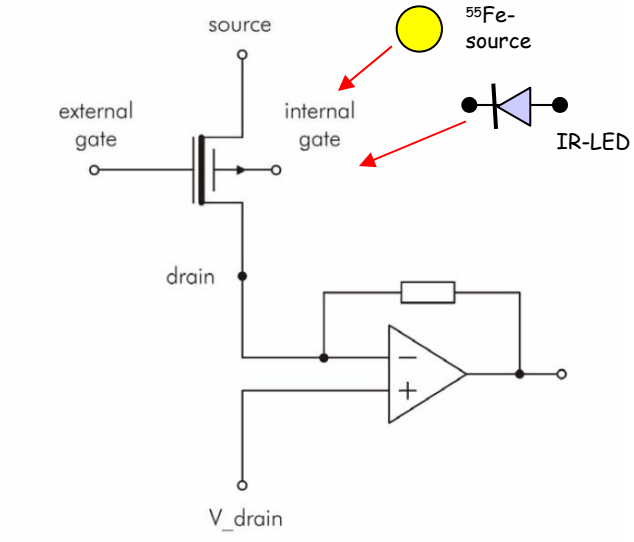
transconductance of the internal gate

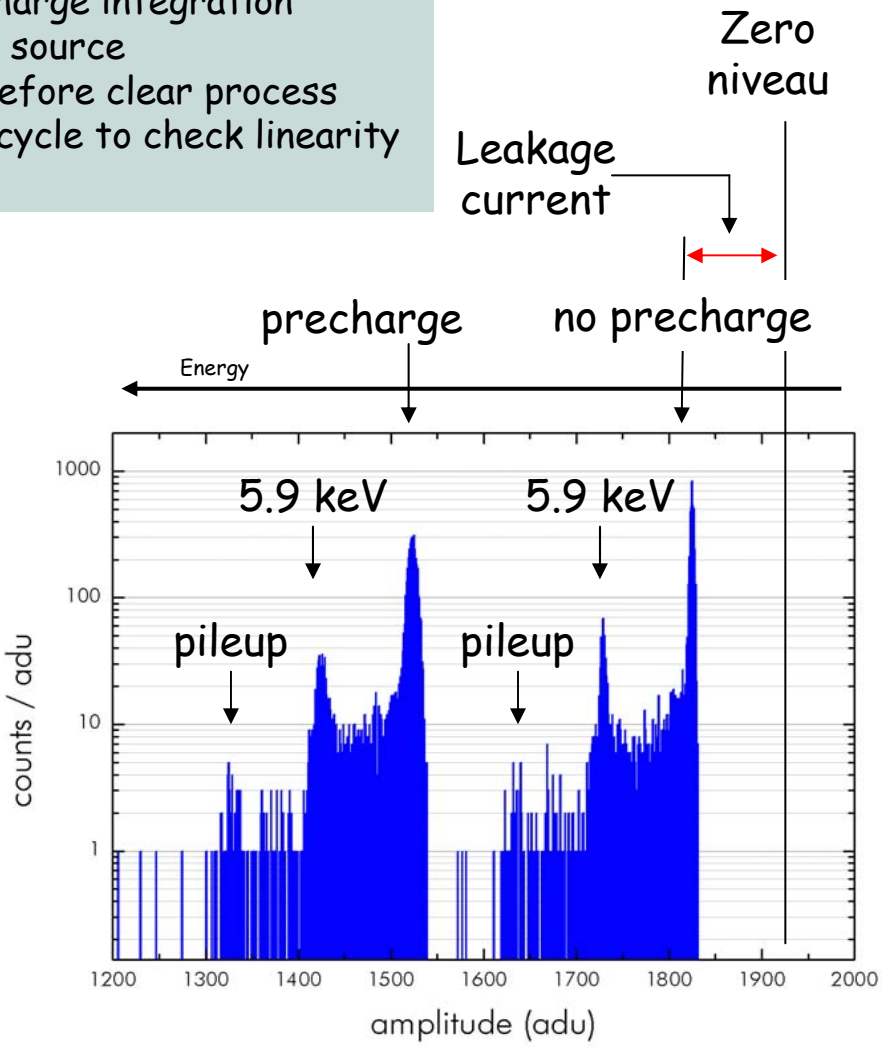
$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2}(V_{GS} - V_{th})$$



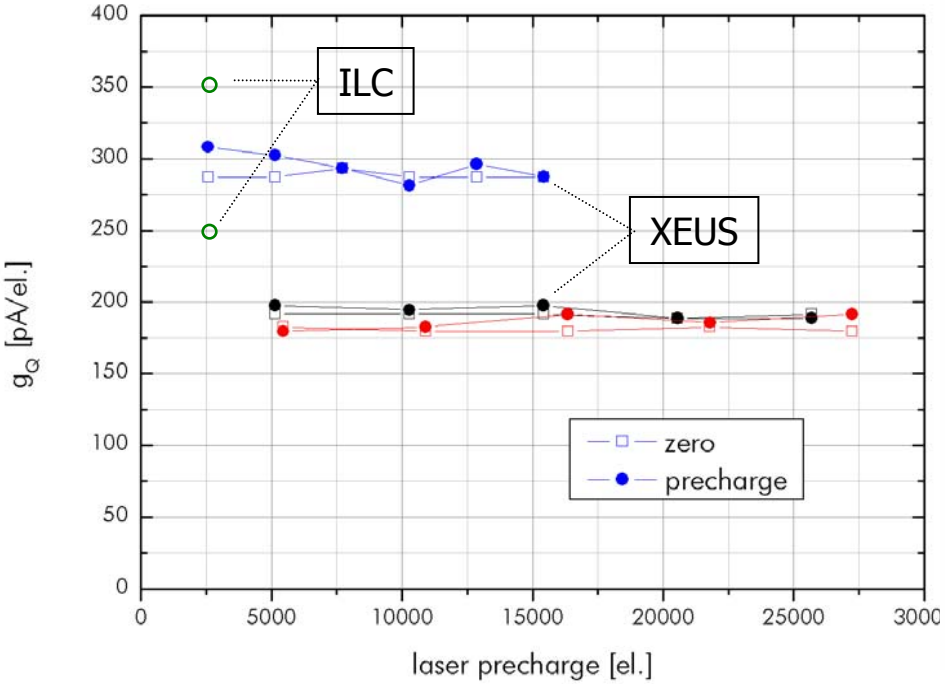
Measurement of g_q

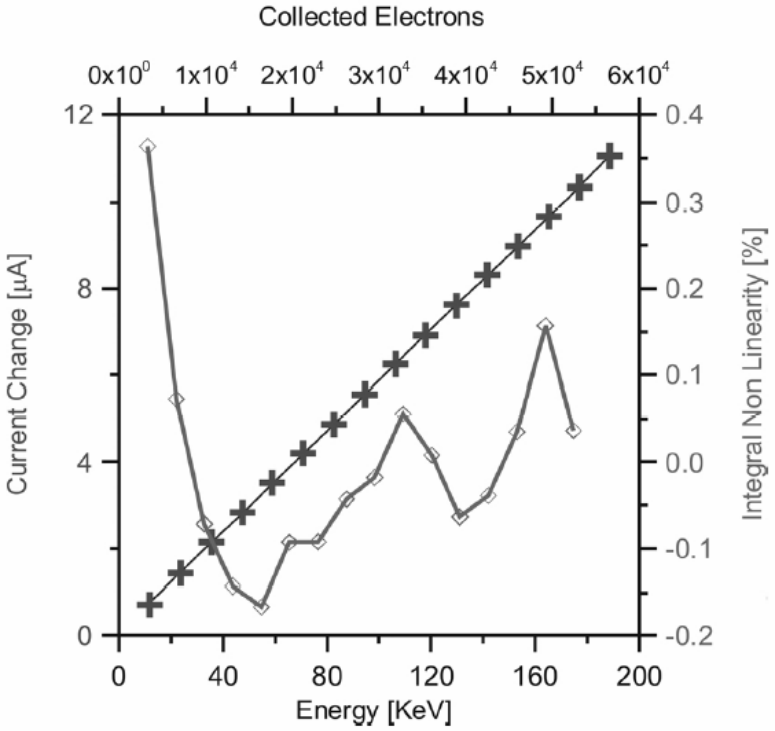
- **Drain readout setup**
- Measurement of g_q in **dynamic mode** using charge integration
- Fixed clear frequency, illumination with ^{55}Fe source
- Sampling output voltage after integration, before clear process
- Additional precharge by laser every second cycle to check linearity
- Result: **Pulse height spectrum**





Measurement of g_q

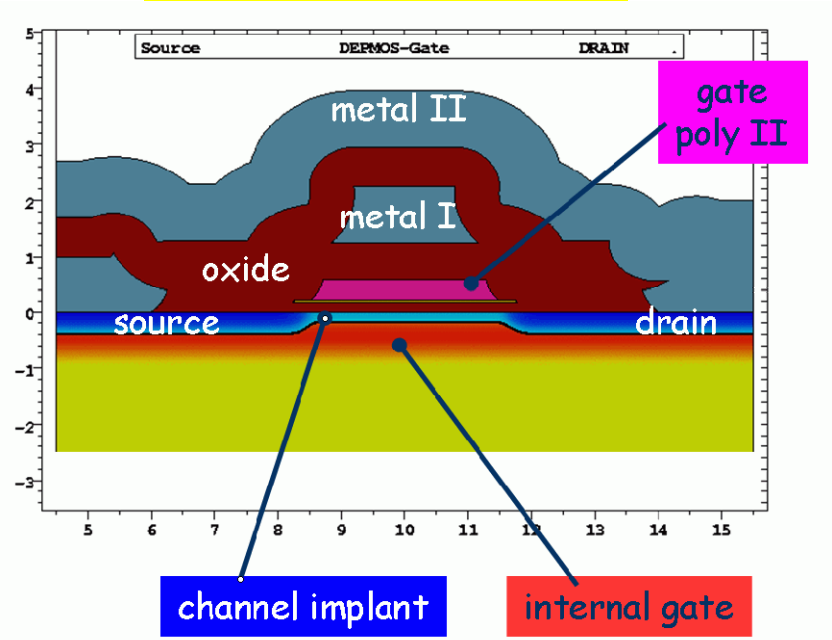


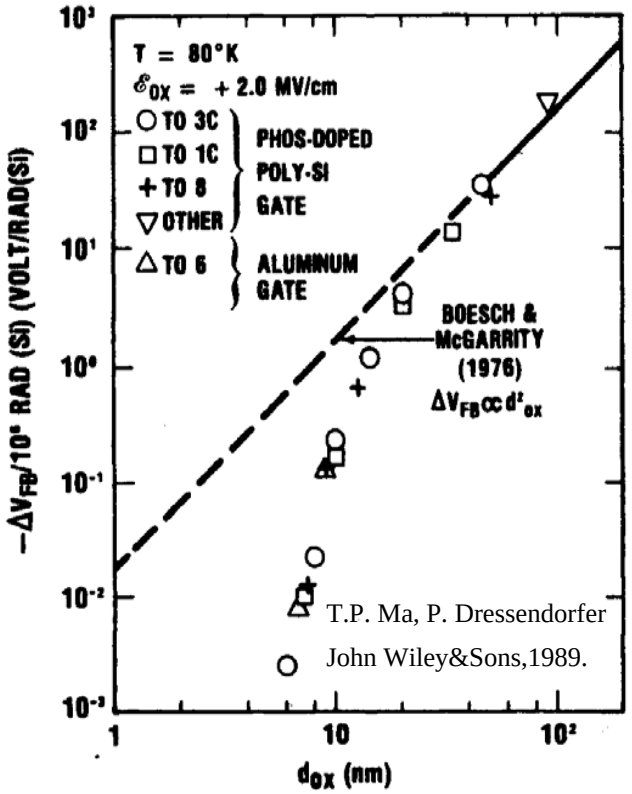


- Measured g_q values meet expectations from simulations
- No dependence on precharge in observed range
- Charge handling capacity $O(10^5)$ electrons

Radiation Effects

Gate Dielectrics t>200nm





T.P. Ma, P. Dressendorfer
John Wiley&Sons,1989.

1. postive oxide charge and positively charged oxide traps have to be compensated by a more negative gate voltage: negative shift of the threshold voltage

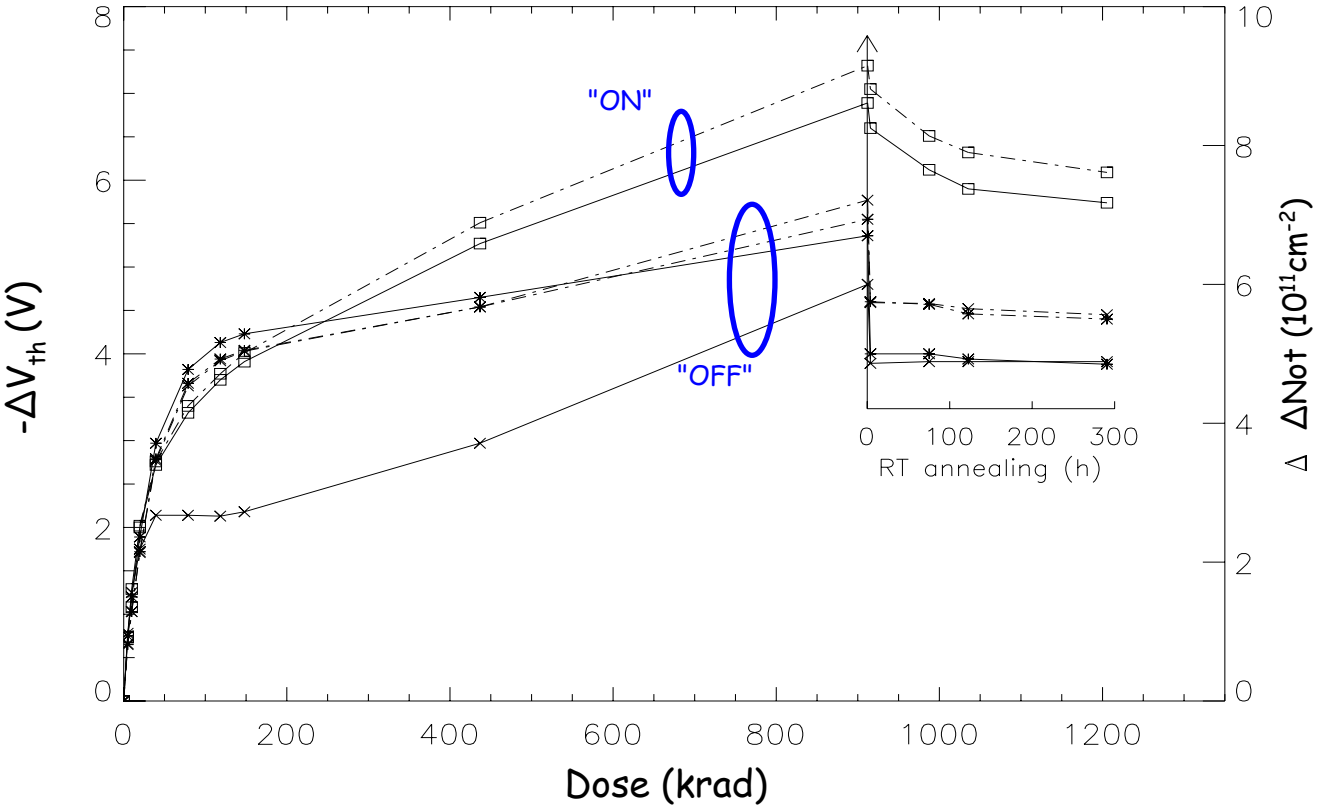
2. increased density of interface traps: higher 1/f noise and reduced mobility (g_m)

Threshold voltage shift

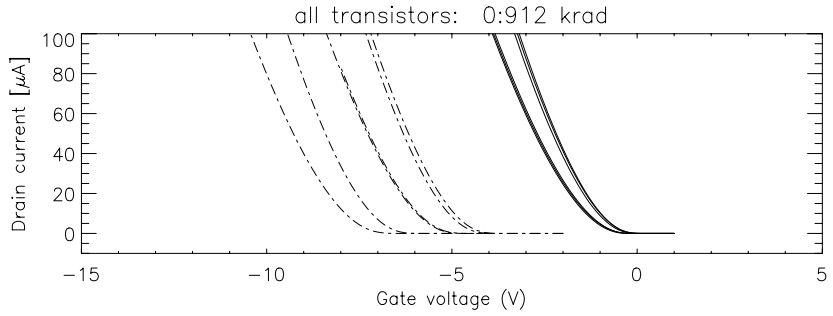
GSF – National Research Center for Environment and Health, Munich

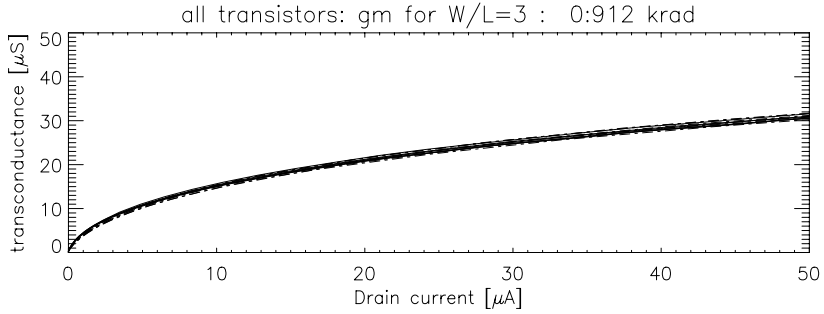
^{60}Co (1.17 MeV and 1.33 MeV)

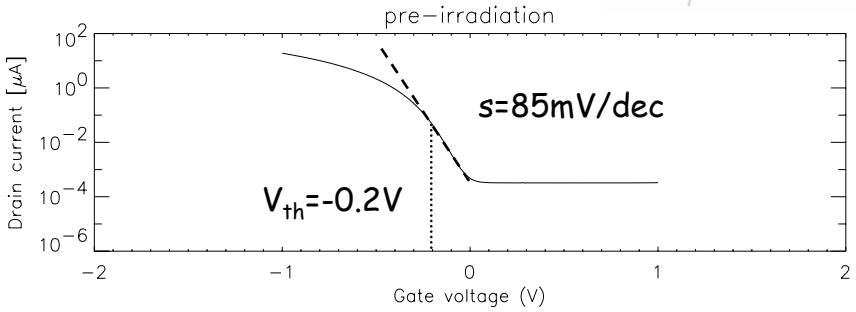
No annealing during irradiation
→ ~ 3 days irradiation
Dose rate: ≈ 20 krad(SiO_2)/h

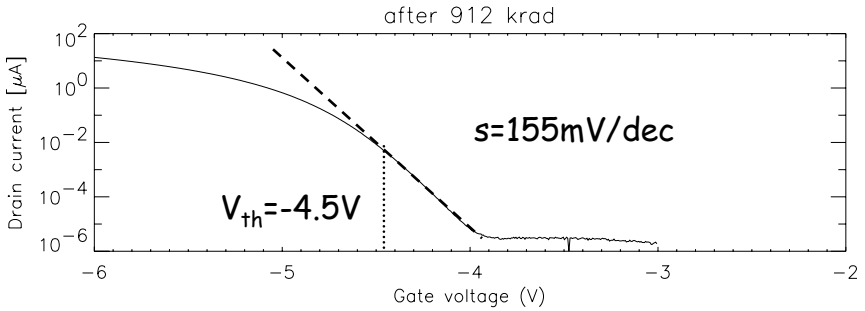


Transconductance and subtreshold slope









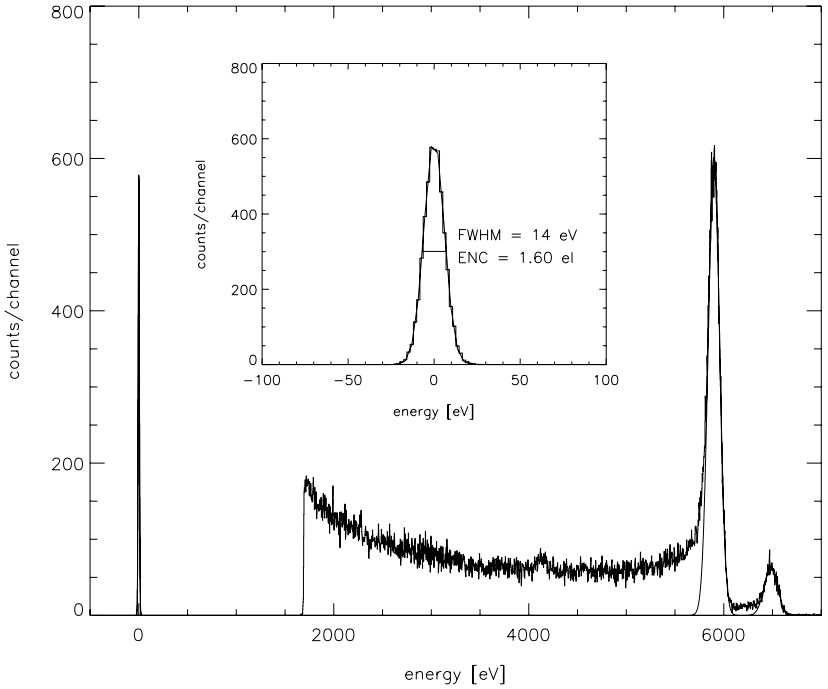
No change in the transconductance g_m

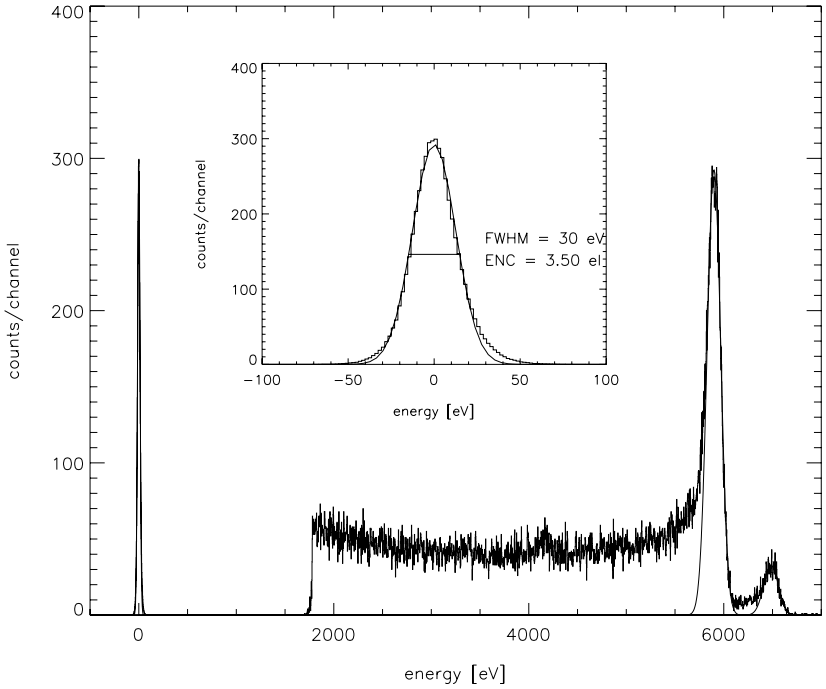
$$N_{it} = \frac{C_{ox}}{kT} \cdot \ln(10) \cdot (s_{D2} - s_{D1})$$

300 krad → $N_{it} \approx 2 \cdot 10^{11}$ cm^{-2}
912 krad → $N_{it} \approx 7 \cdot 10^{11}$ cm^{-2}

Literature:
After 1Mrad 200 nm (SiO_2):
$N_{it} \approx 10^{13}$ cm^{-2}

^{55}Fe Spectrum (single pixel)





non-irradiated

V_{thresh}≈-0.2V, V_{gate}=-2V

I_{drain}=41 μA

time cont. shaping τ=10 μs

Noise ENC=1.6 e^- (rms)

at T>23 degC

912 krad ^{60}Co

V_{thresh}≈-4.0V, V_{gate}=-6.0V

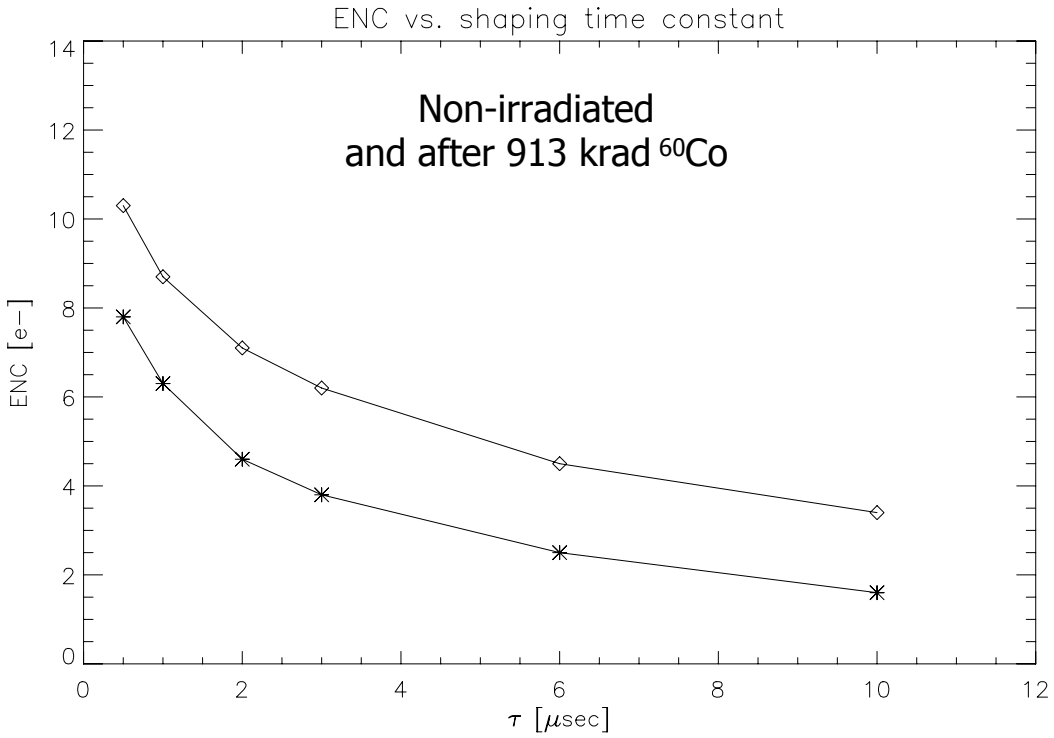
I_{drain}=40 μA

time cont. shaping τ=10 μs

Noise ENC=3.5 e^- (rms)

at T>23 degC

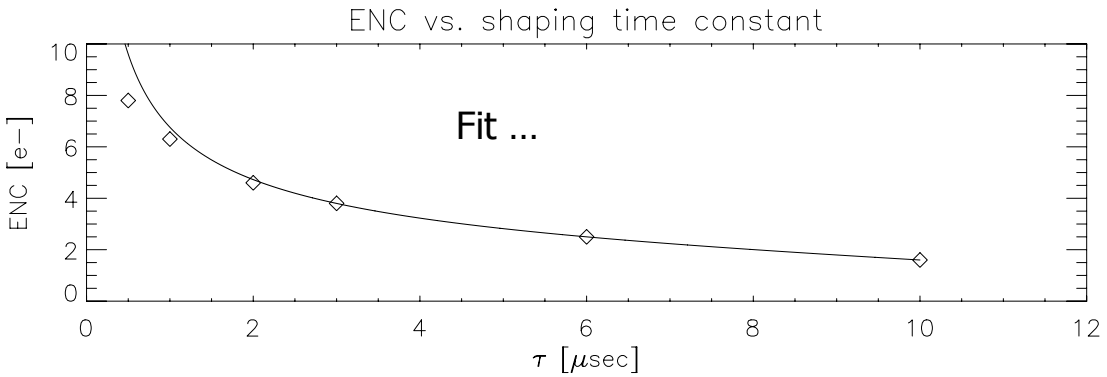
Noise vs. shaping time τ

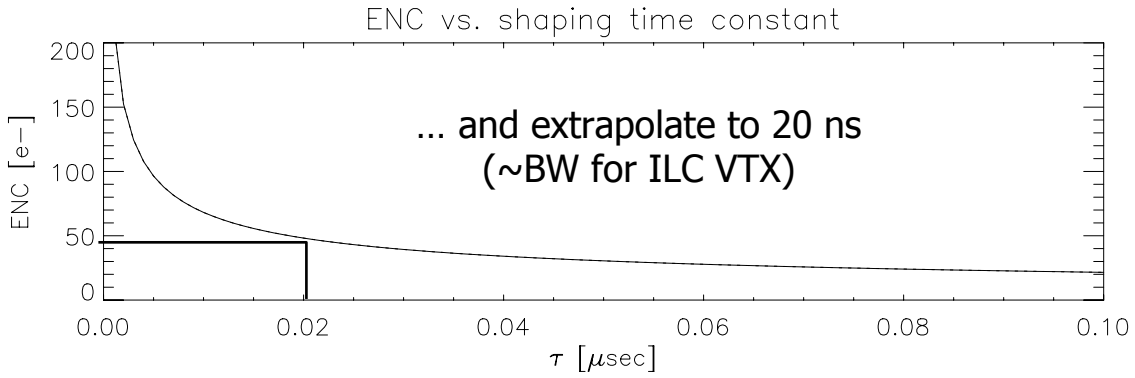


$$ENC = \sqrt{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau} + 2\pi a_f C_{tot}^2 A_2 + q I_L A_3 \tau}$$

Therm. noise | 1/f | I_L

Noise vs. shaping time τ

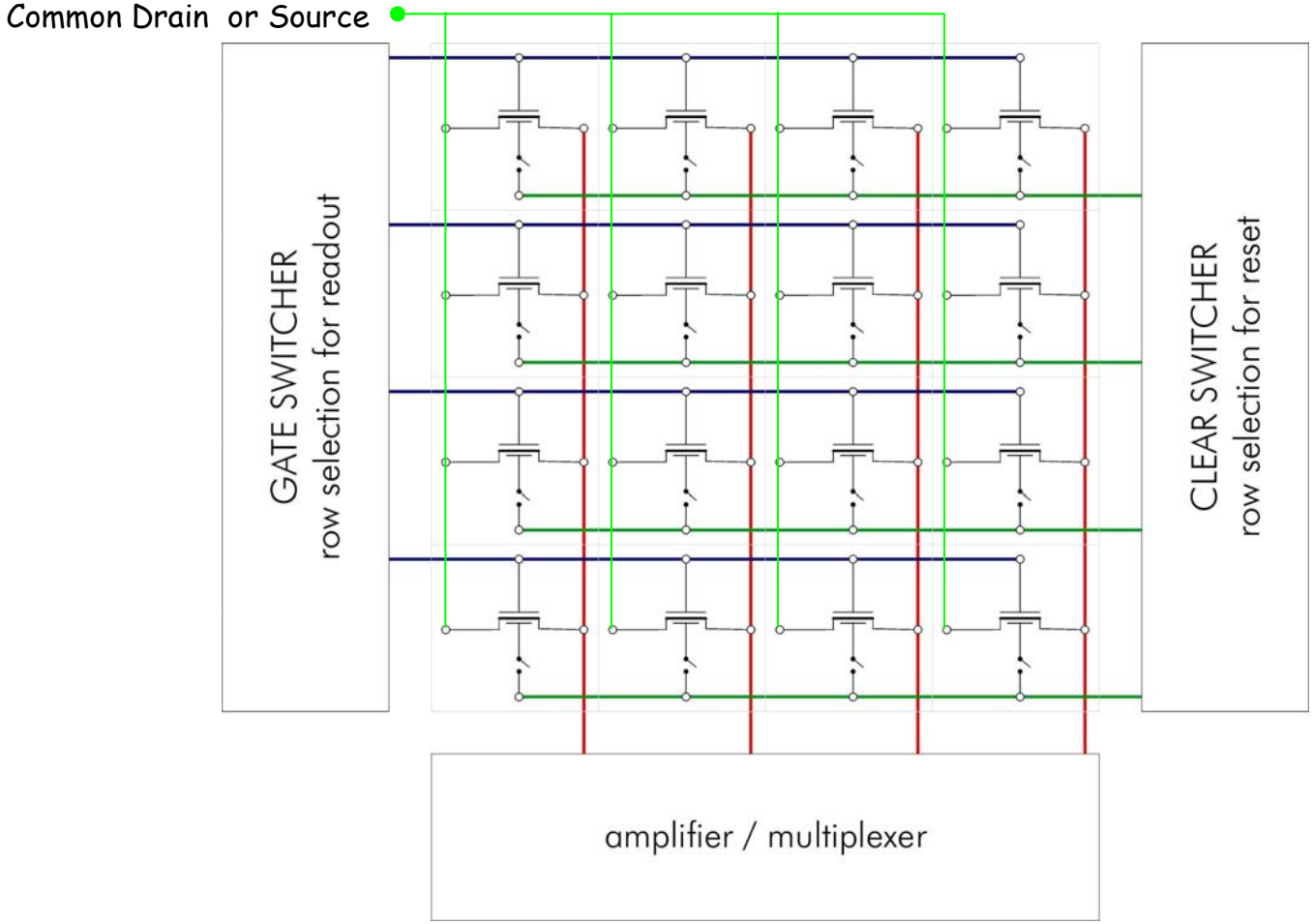




$$ENC = \sqrt{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau} + 2\pi a_f C_{tot}^2 A_2 + q I_L A_3 \tau}$$

Therm. noise | 1/f | I_L

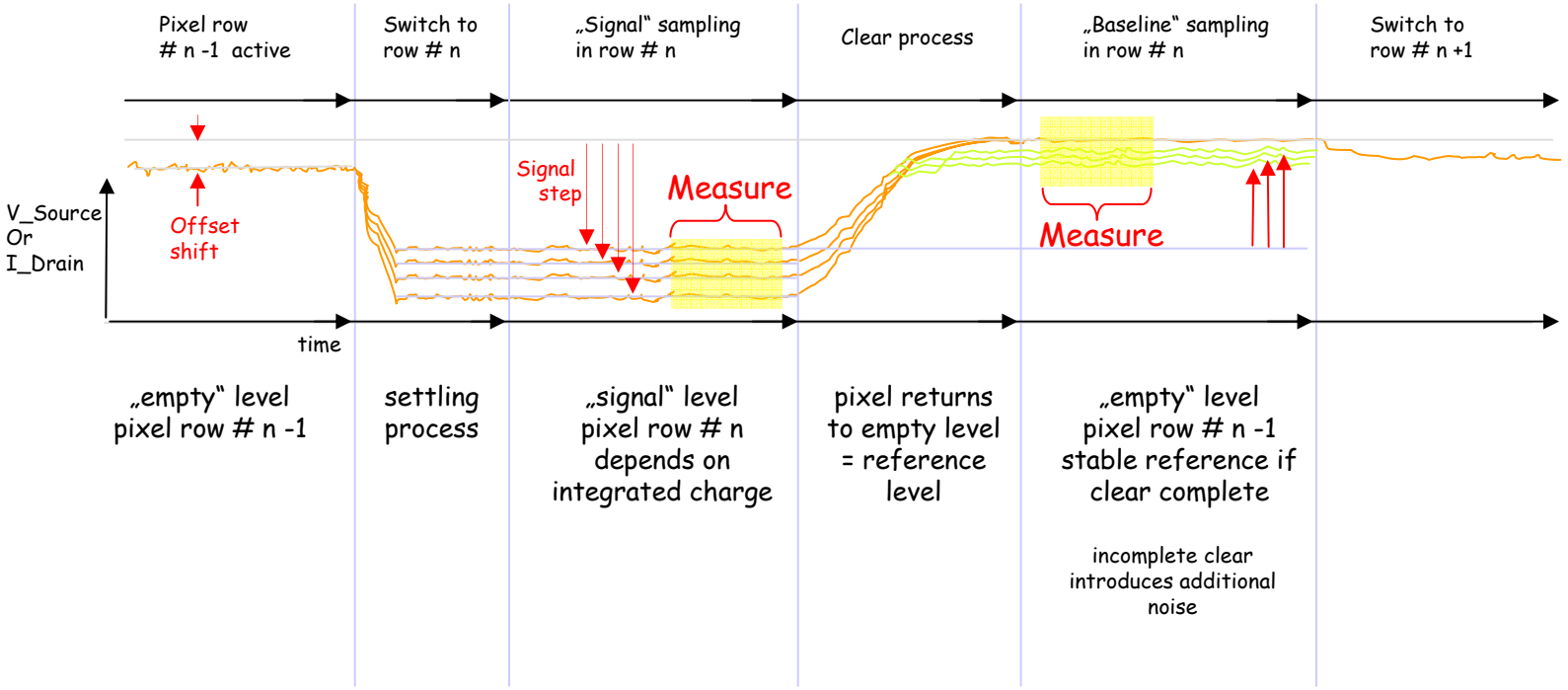
Matrix integration



Auxiliary ASICs needed:

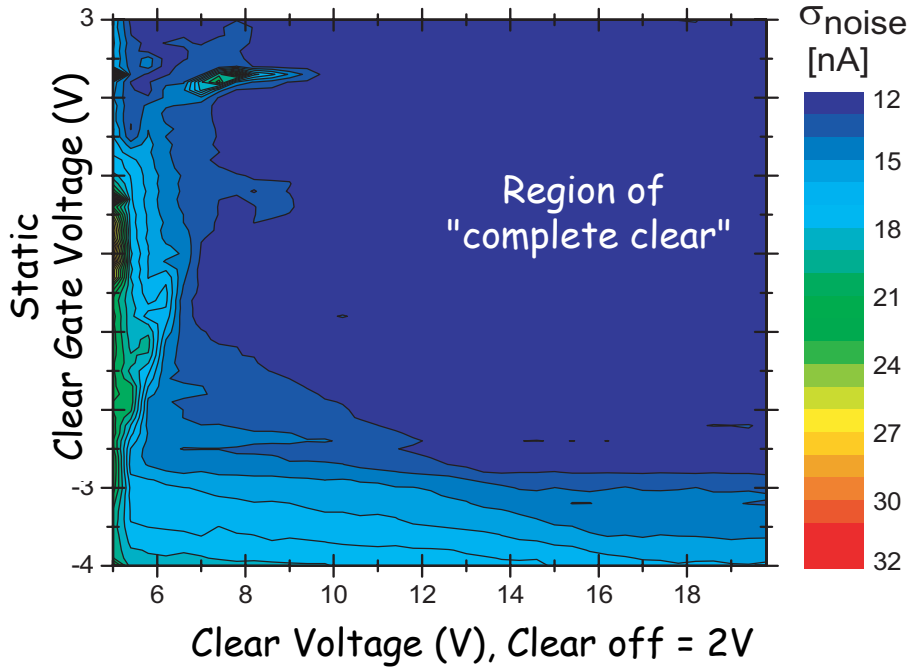
- Switching circuitry (for rows) → "SWITCHER"
- Analog front-end circuit (for columns) → "CAMEX" or "CURO"

Matrix signal



Clear Efficiency

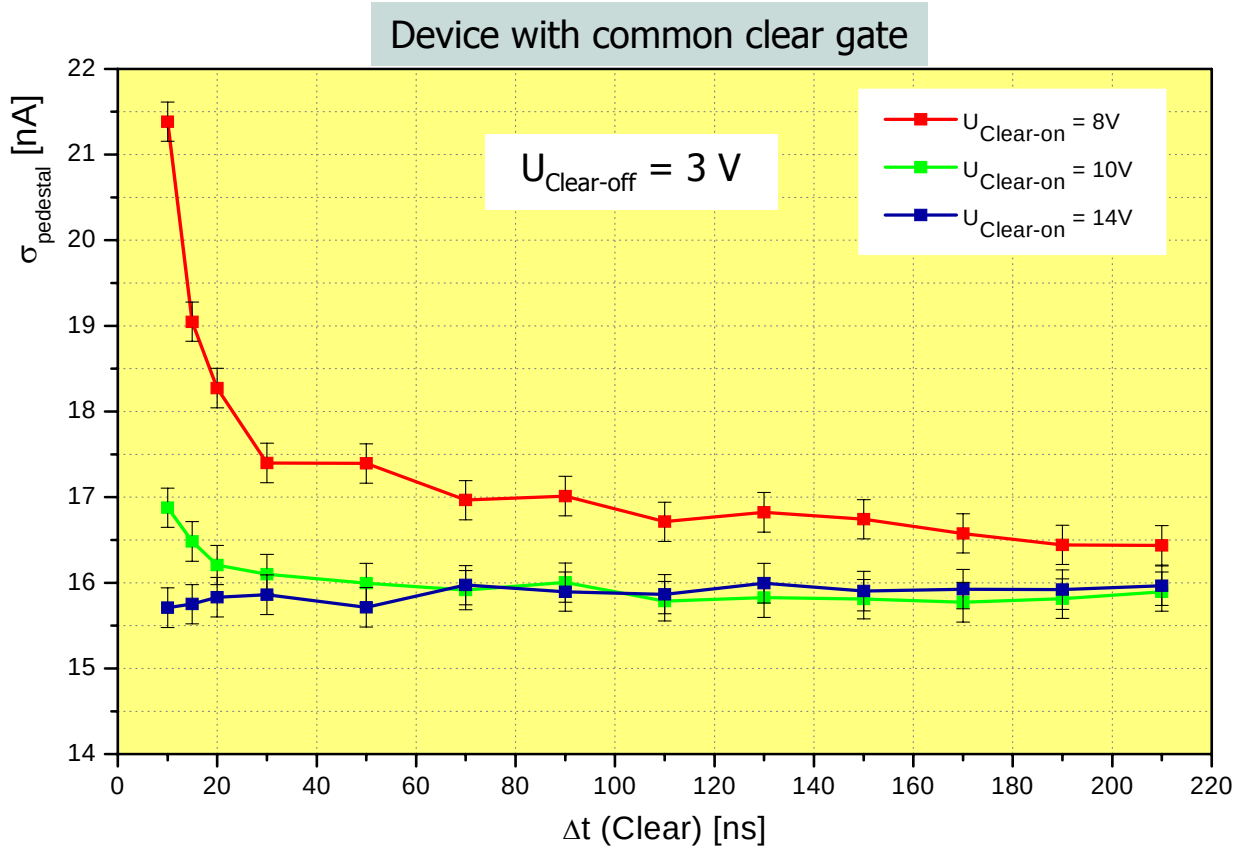
- Study mini matrix devices in laser setup
- Scan wide parameter space of Clear Gate and Clear Voltage
- Study various designs, geometries (length of clear gate) and operating conditions (static or clocked clear gate)



Complete clear achieved with static clear gate !
Required voltages are small (5-7V) – very important for future SWITCHER!

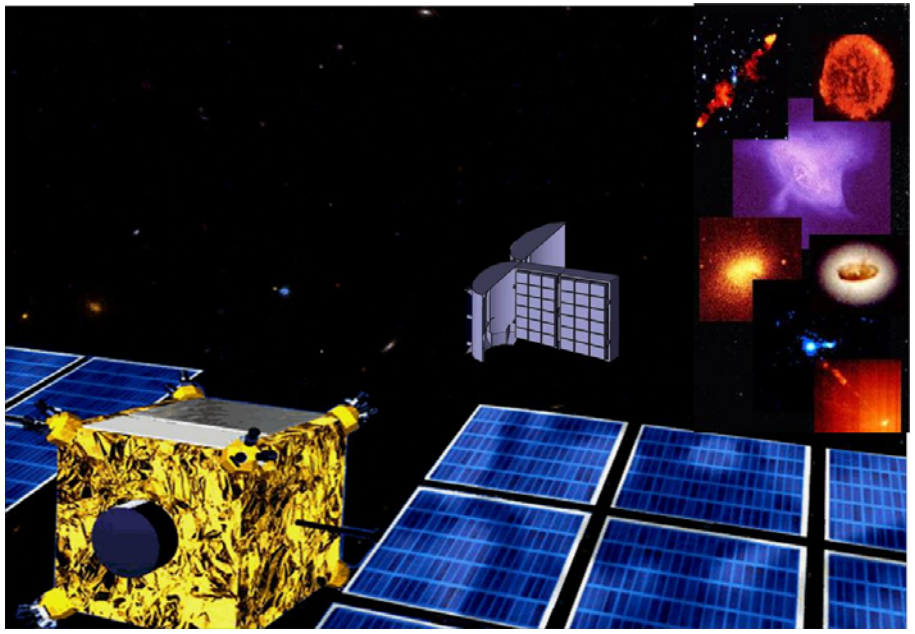
Fast Clearing

- Study clear efficiency for short clear pulses



Complete clear in only 10-20 ns @ ΔV_{clear} = 11-7 V

The XEUS mission



Status:
Mission under assessment

:- Payload definition completed

:- PDD (strawman payload)

:- Feasibility study ← Now!

:- Decision: end 2006 / beg. 2007

⋮

Launch ~ 2015+

Mission concept:

- Increased focal length (35m - 50 m)
- X-ray telescope consisting of two satellites
- Energy range: 0.1 - 40 keV
- Mirror area $2m^2$ at 6keV and $5m^2$ at 1keV

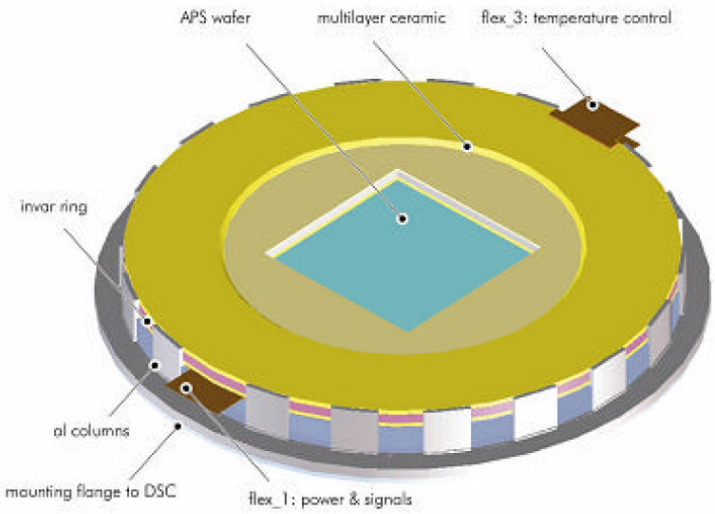
Baseline instrumentation

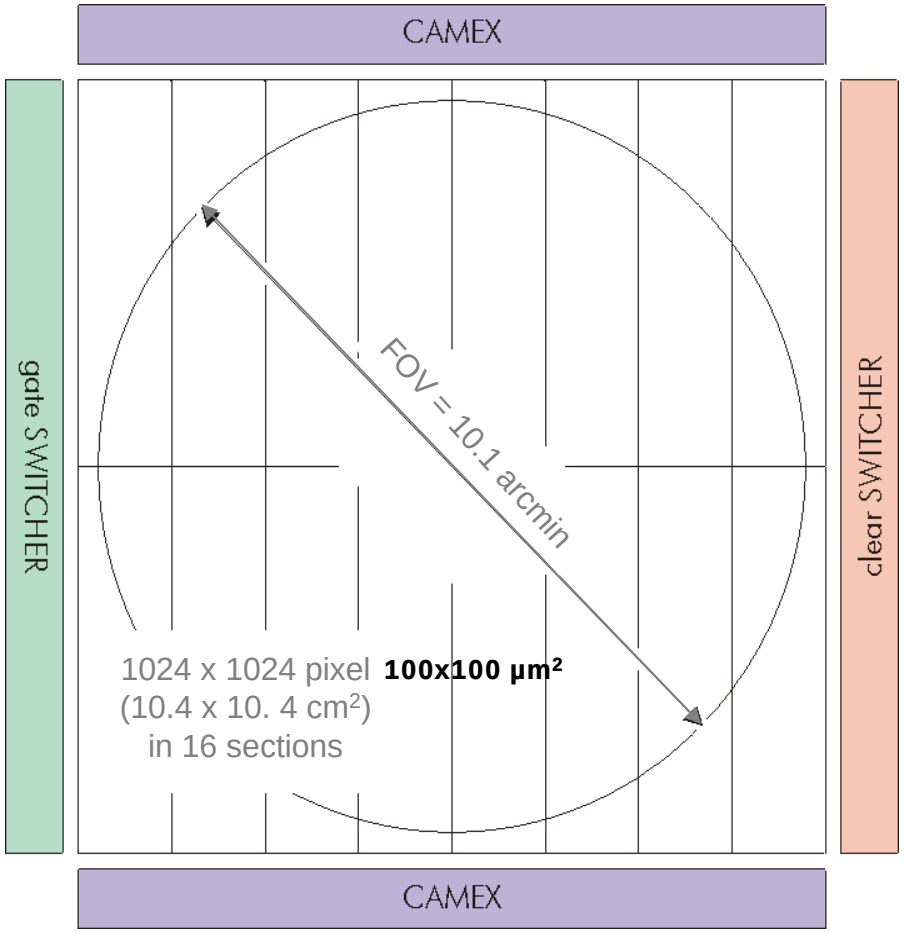
Core payload complement:

1:- Wide Field Imager: DEPFET APS

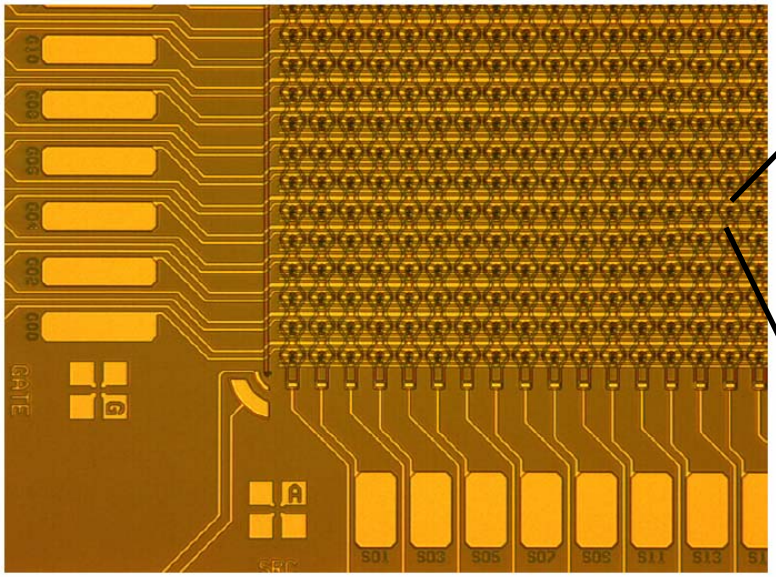
2:- Narrow Field Imager

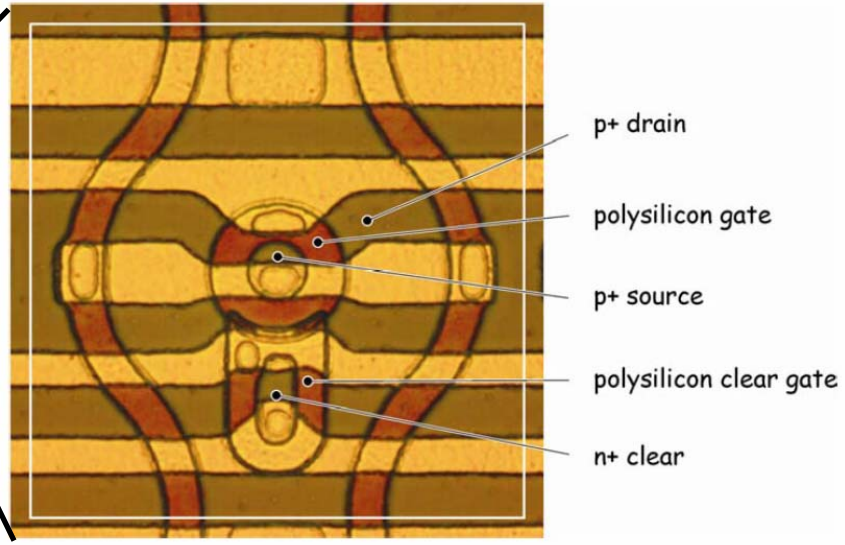
option 1: superconducting tunnel junctions at 250 mK
option 2: micro calorimeter at 50 mK





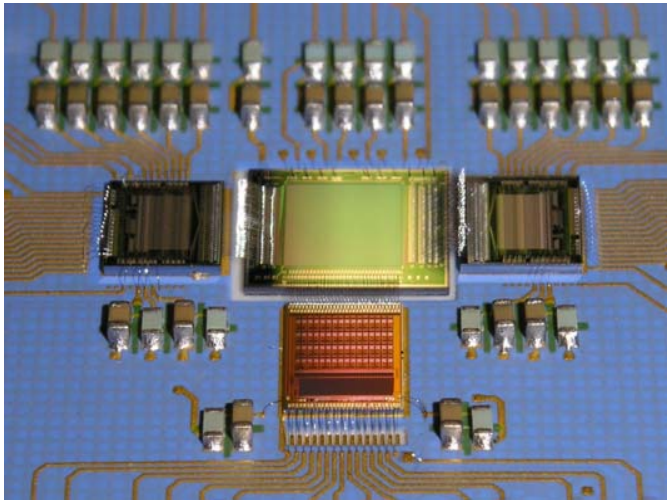
XEUS prototype



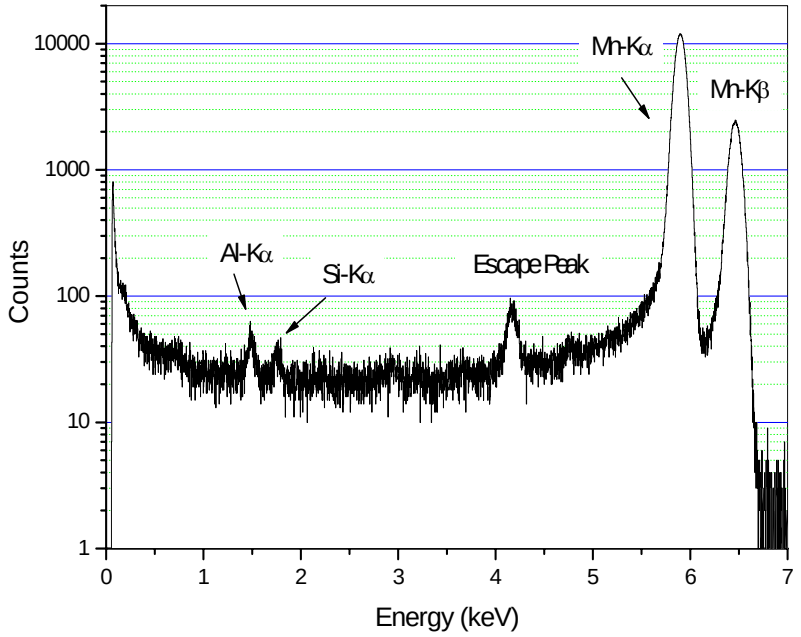


DEPFET XEUS Prototype

- 75x75 μm^2 pixel
- 64x64 pixel matrix



XEUS prototype - Spectroscopy



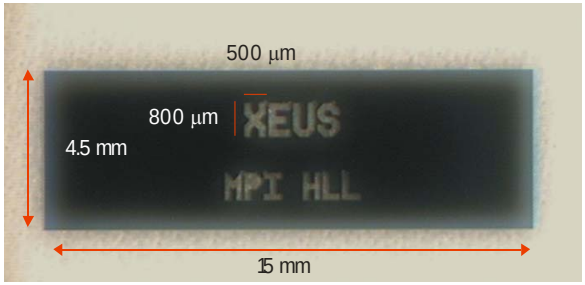
Energy resolution:
126 eV FWHM @ Mn-Ka Line
corresponding to 4.9 e^- ENC

Conditions

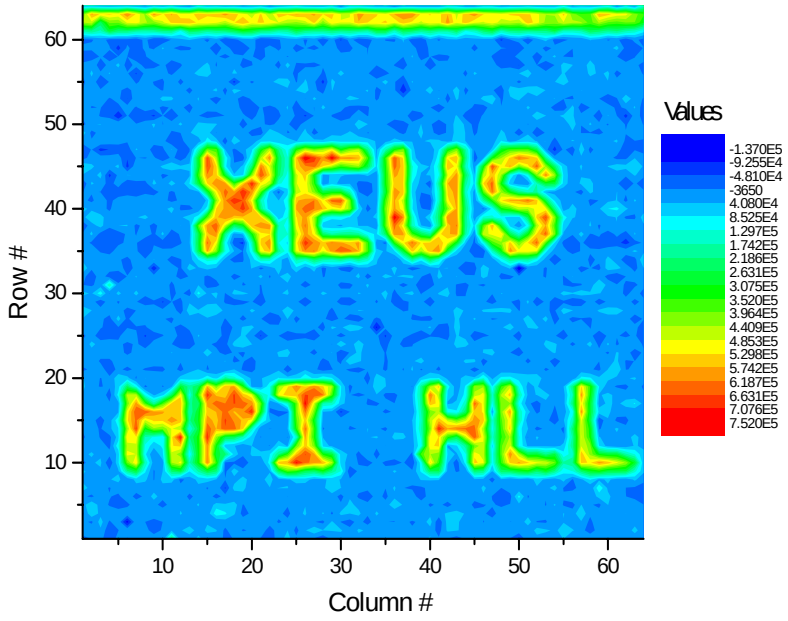
- Nitrogen atmosphere
- Temperature: -50° C
- Frame rate 300 Hz
- Pixel current 30 μA
- Line processing time 25 μs
- "frontside" illumination

Imaging with ^{55}Fe

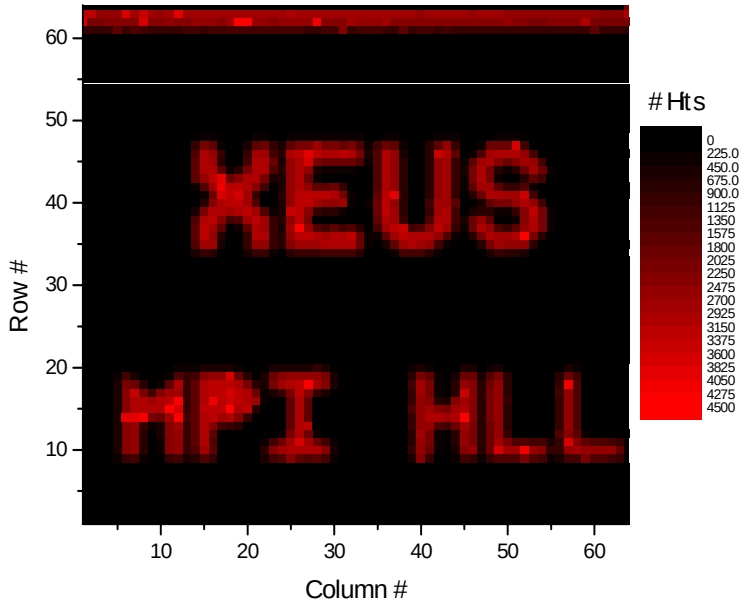
- Illumination from backside
- Baffle: 300 μm thick silicon
- Minimal structure size: 150 μm
- Exposure ca. 100000 frames



- Contour plot from ADU maps



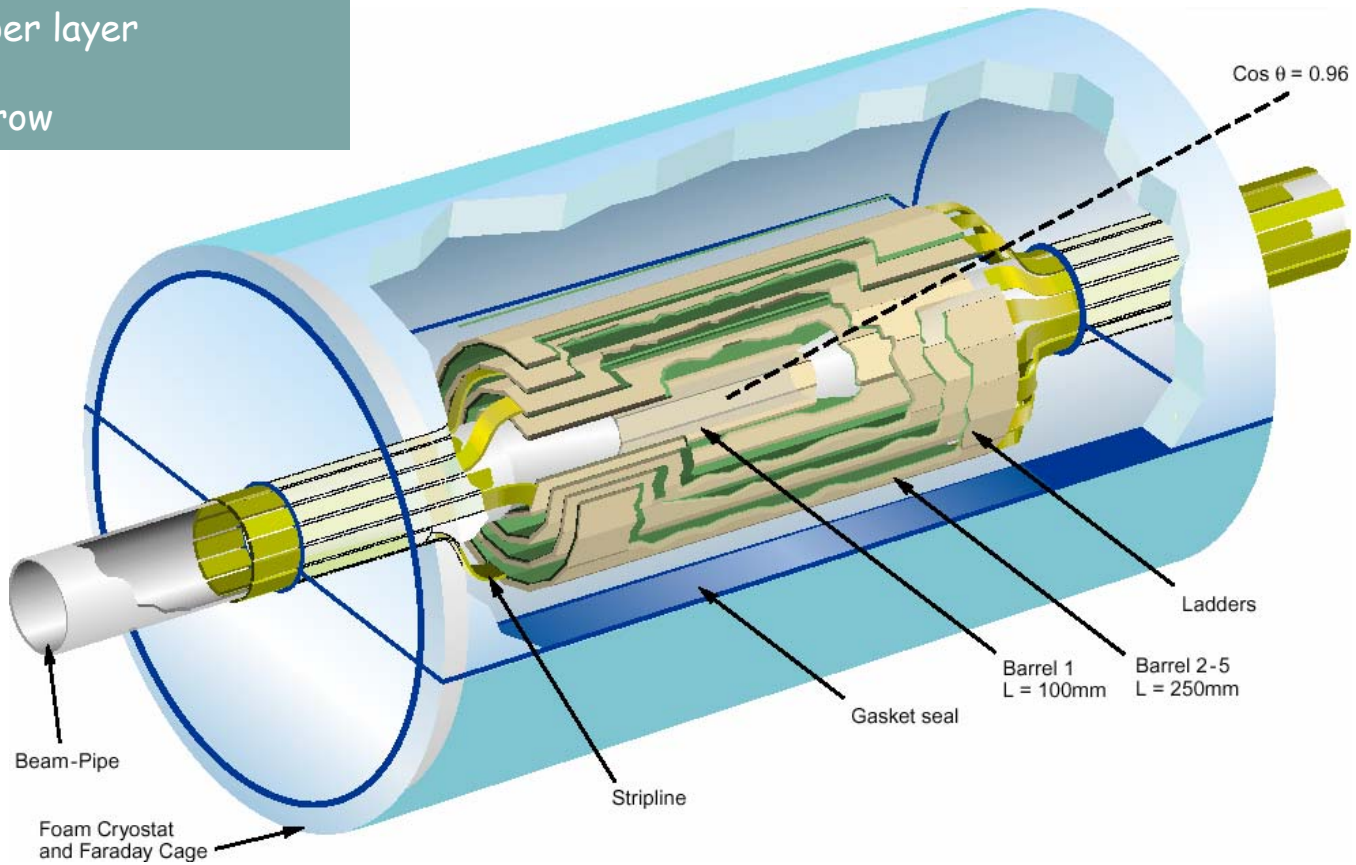
- Hitmap with 100 ADU threshold



Generic Layout of the ILC Vertex Detector

- $\sigma_d \leq 5\ \mu m \oplus 10\ \mu m/(p \cdot \sin^{3/2}\Theta)$
- pixel size: 20-30 μm
- low mass: 0.1 %Xo per layer
- fast(!): 20 - 40 ns/row

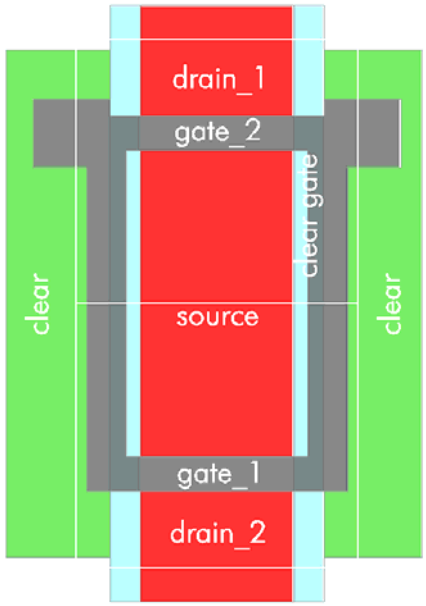
TESLA TDR Design

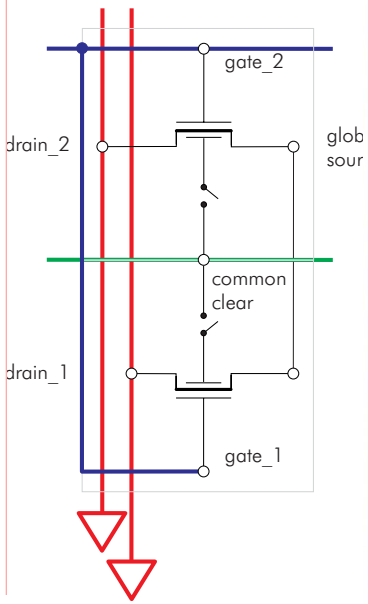


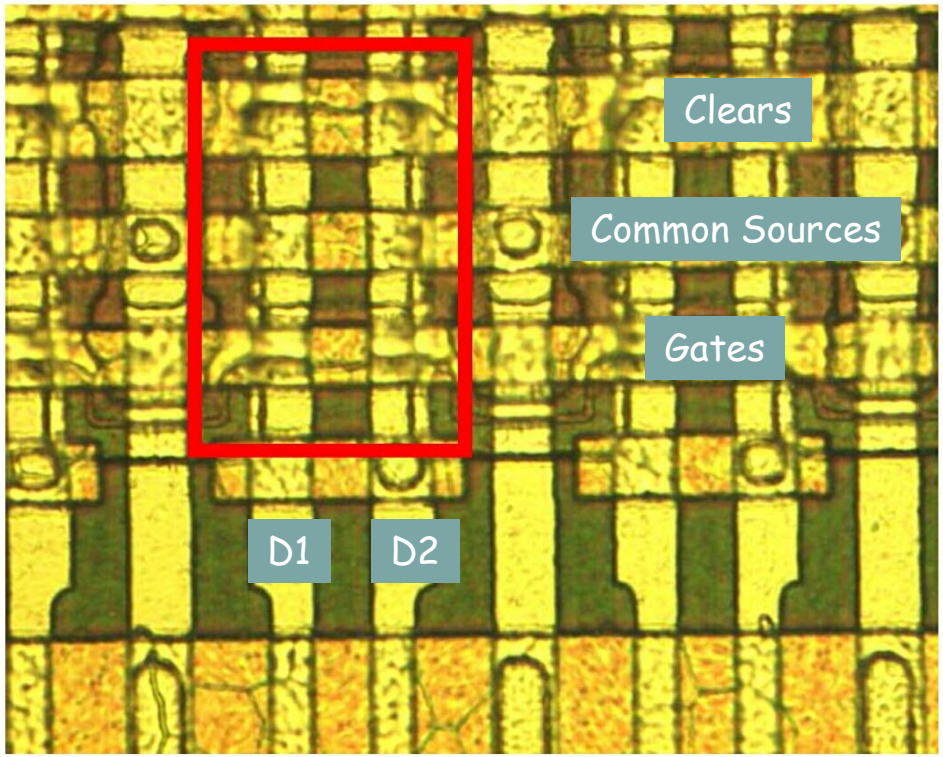
1st layer module: 100x13 mm², 2nd-5th layer : 125x22 mm² ➔ Σ120 modules

Compact linear DEPFETs

smallest pixel cell 22.5 x 36 μm²
limited by technology: smallest feature size ≈2μm

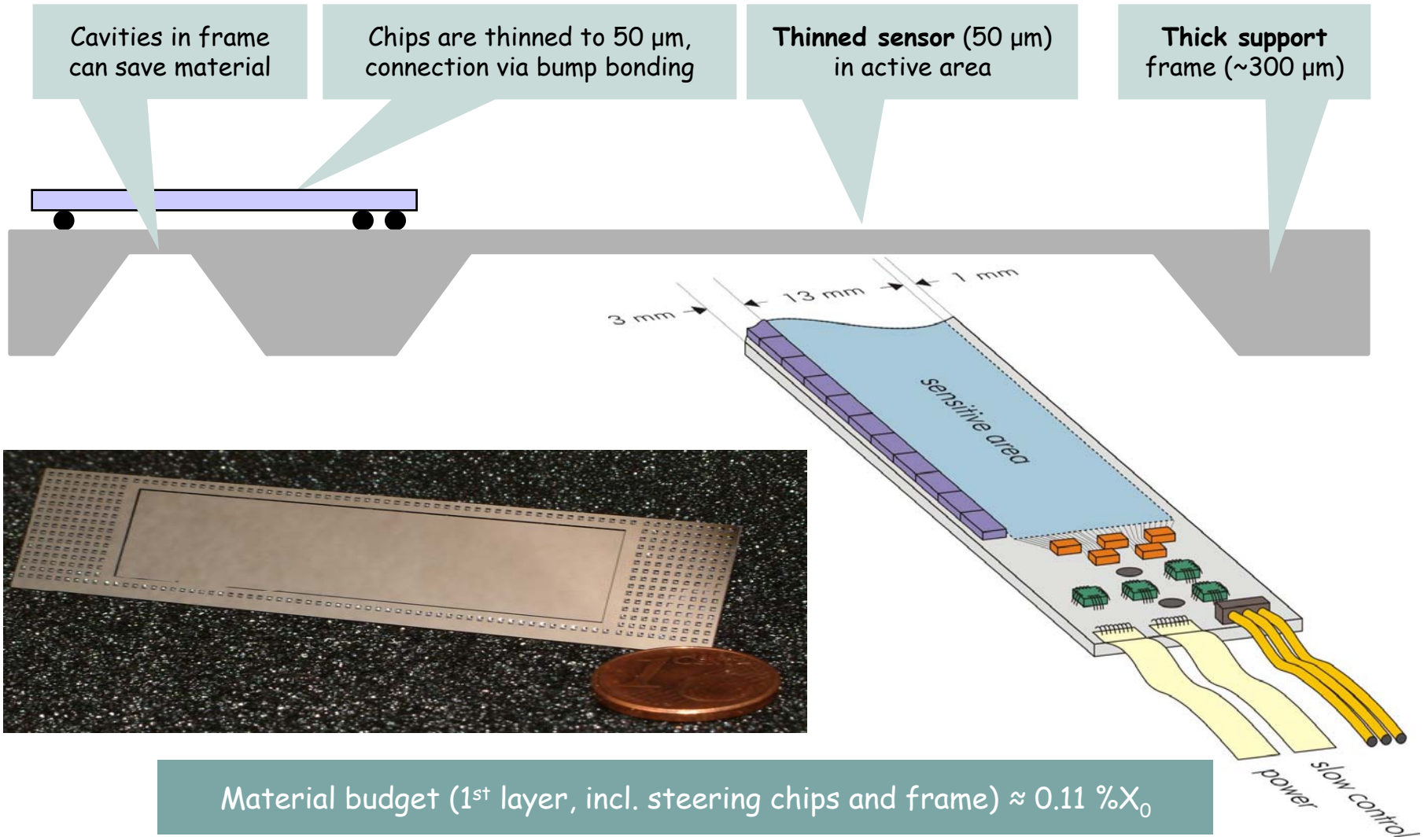






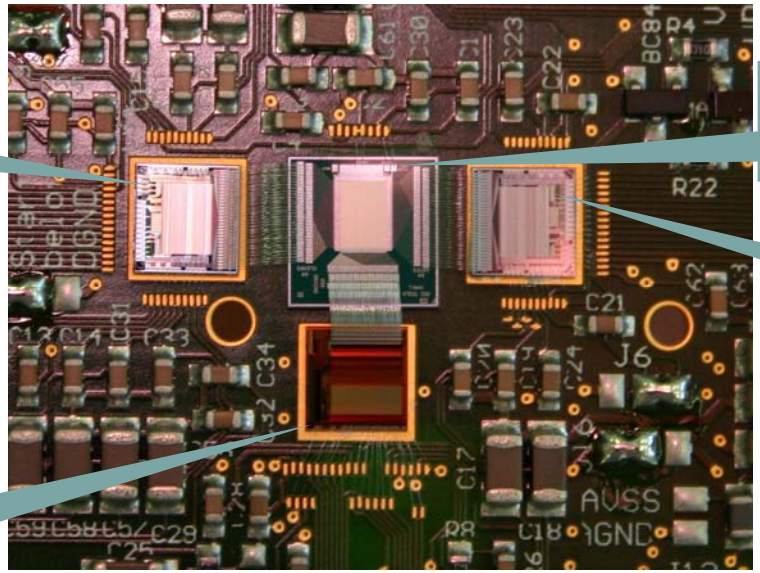
Double pixel cells:
reduces the required read out speed by 2 → doubles the number of readout channels

Module Concept: "all-silicon module"



Material budget (1st layer, incl. steering chips and frame) ≈ 0.11 %X_0

ILC Prototype System



Gate Switcher

DEPFET Matrix
64x128 pixels, 36 x 28.5μm^2

Clear Switcher

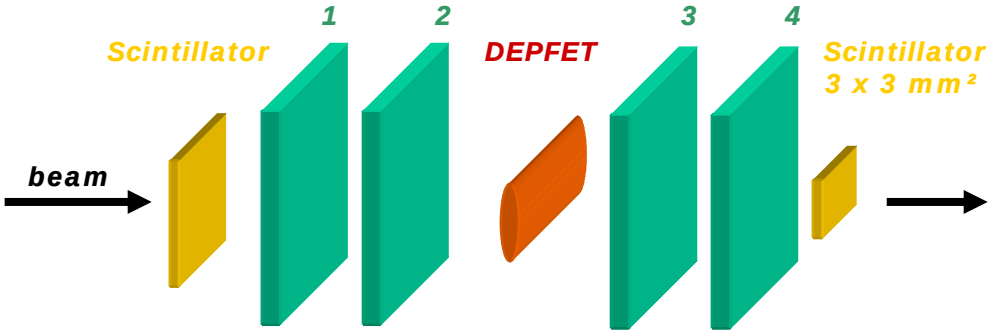
- 2 analog MUX outputs with
- 64 channels each
- Can switch up to 25 V
- 0.8μm AMS HV technology
- radhard version in progress

Current Readout CUROII

- current based 128 channel readout chip
- 50 MHz band width in the f/e
- On-chip pedestal subtraction by switched current technique (CDS)
- Real time hit finding and zero suppression
- 0.25μm CMOS technology (radhard design)

See Poster 231, Marcel Trimpl:
"A DEPFET Pixel System for the ILC Vertex Detector"

Testbeam at DESY, Jan. '06



5 Hybrids with different matrices under test
all 450 µm thick

-: DESY test beam with 1- 6 GeV e-

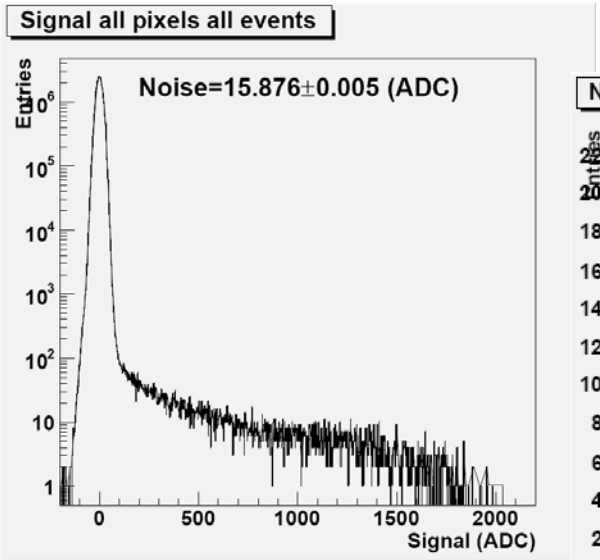
-: Bonn ATLAS telescope system:
double sided strip detectors, 300µm
pitch 50 µm (no intermediate strips)

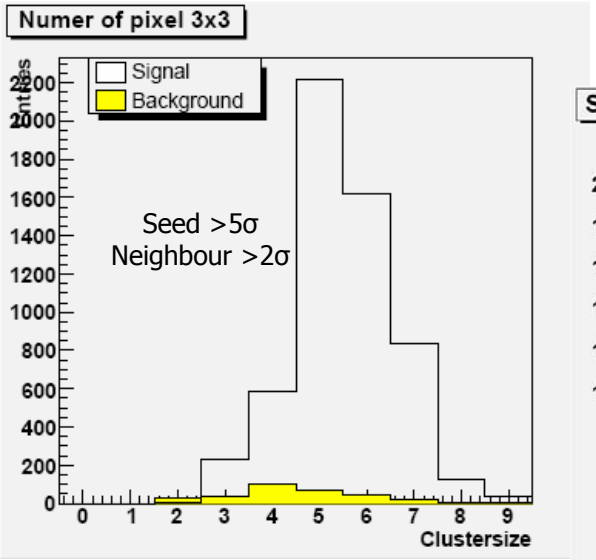
Name	Wafer	Type	Pixelsize (μm)
Hyb1B	W09 O03	CCG nonHE rec small	33×23.75
Hyb1A	W11 J12	CCG HE rec small	33×23.75
Hyb2A	W11 B03	CCG HE rec small A	36×22
HybMun1		CCG nonHE rec small	33×23.75
HybGCG		GCG nonHE	36×28.5

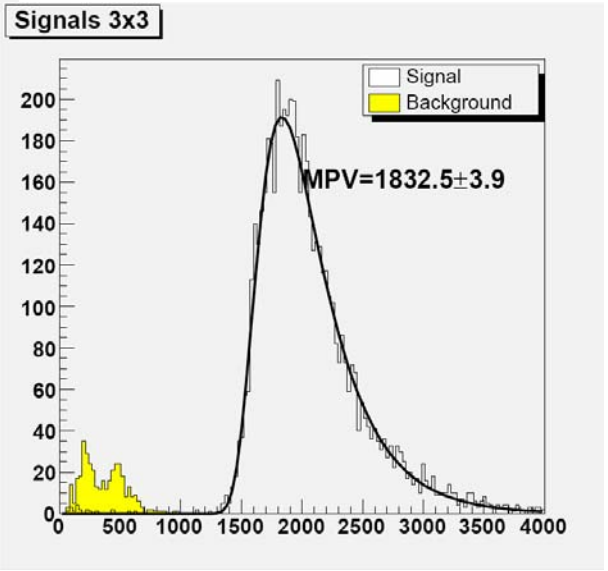
-: bias scans (→cluster size)
-: energy scans (→ resolution)
-: different readout modes…

Some results →

Testbeam at DESY, Jan. '06







- Clock 50 Mhz … but …
- Read all channels (no zero suppression)
- ~ 800 µs/frame (64 rows) → ~ 12 µs/row
- Sample-clear-sample: ~ 240 ns
- Clear duration 20ns

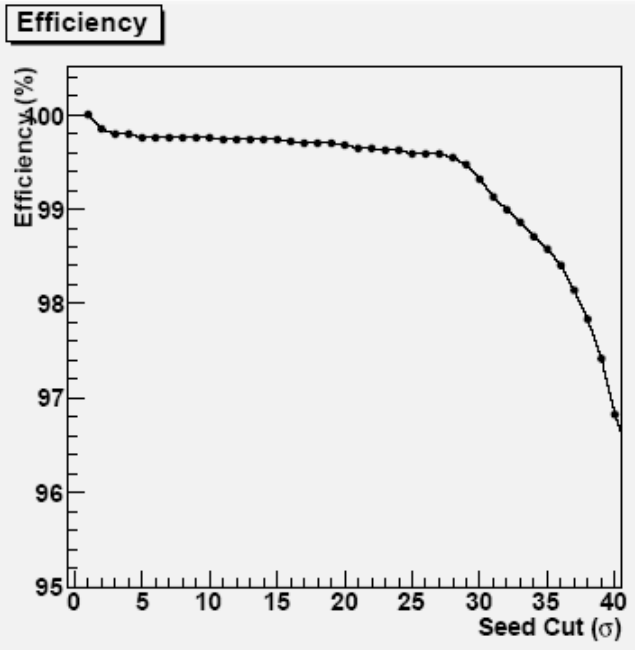
- S/N ≈ 114 (for 450 µm sensor!)
- Noise about 250 - 300 e- ENC

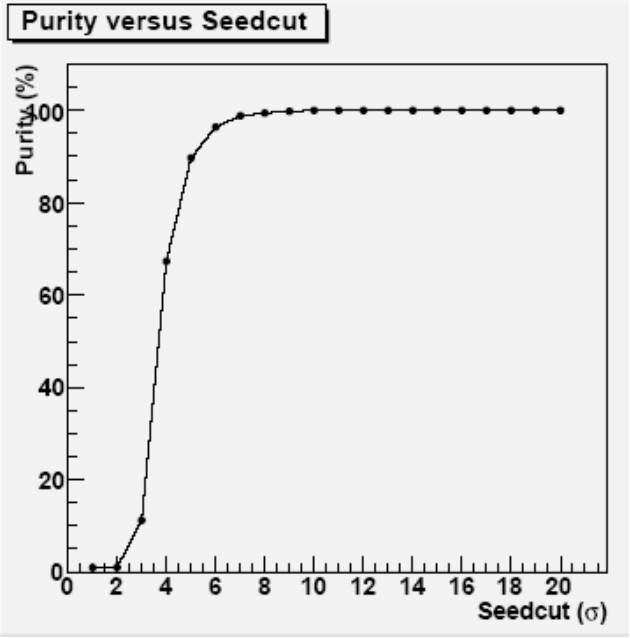
Usual suspects: system x-talk

CURO, external I2V converter…

There is still room for improvement

Efficiency & Position resolution





$$\textbf{Efficiency} = \frac{\text{Number of tracks with cluster}}{\text{Total number of tracks}} \qquad \textbf{Purity} = \frac{\text{Number of clusters with track}}{\text{Total number of clusters}}$$

For 5 σ seed cut

- Efficiency ≈ 99.8%
- Purity ≈ 99.6 %

After corrections for MS (6GeV electrons!!)

Position resolution about 3 - 5 μm

(for 33x23.75 μm^2 pixels)

In Summary....

..... there is so much more to be say and to present but I have to stop here.

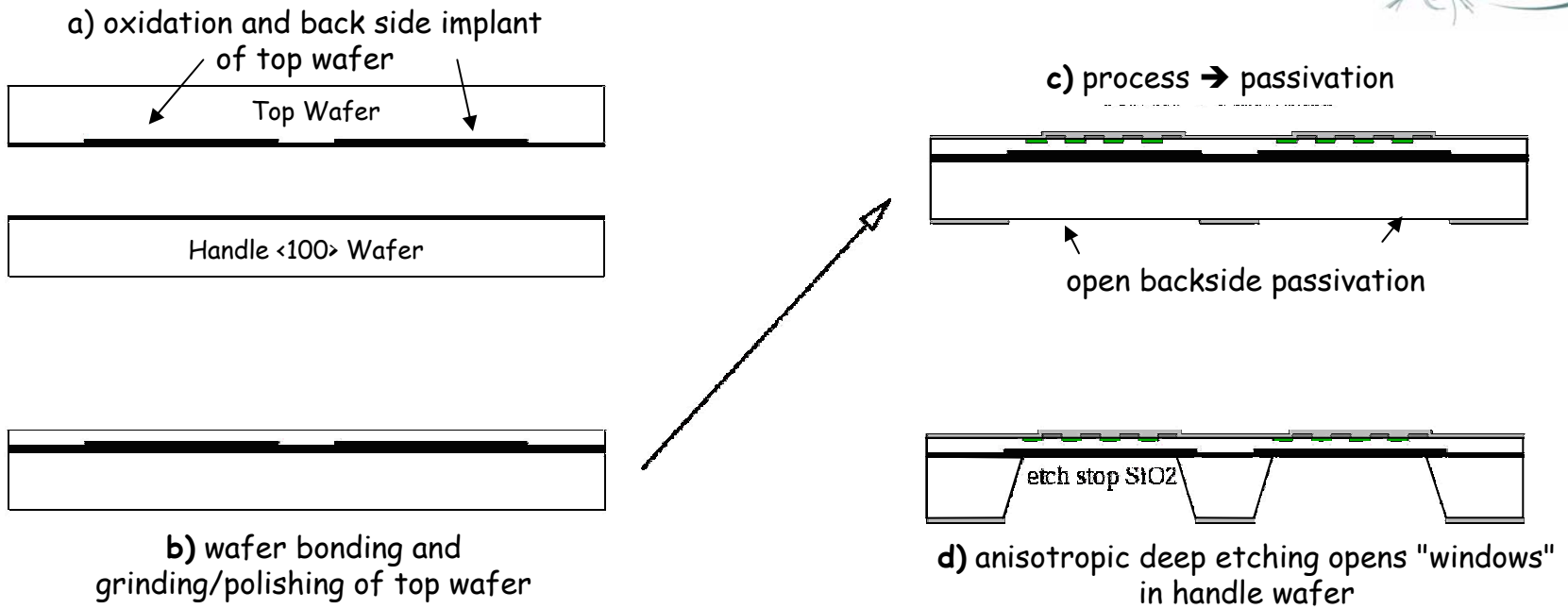
The new generation of DEPFETs developed for

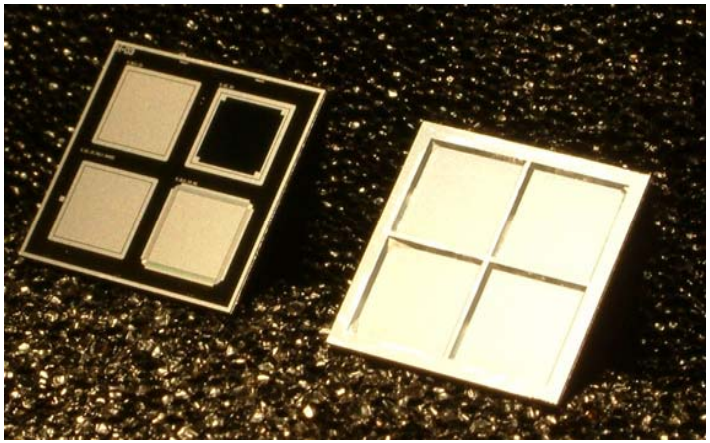
- space based X-spectroscopy and imaging
- vertexing at future collider experiments

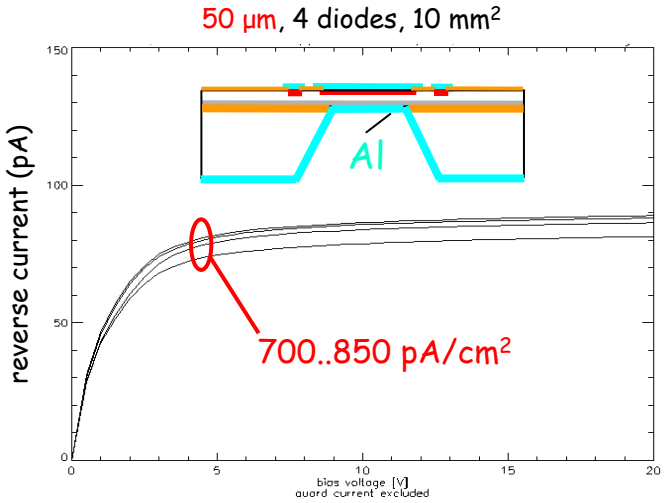
is ready to go for the next round, i.e. the production of larger matrices in 2006

Backup slides

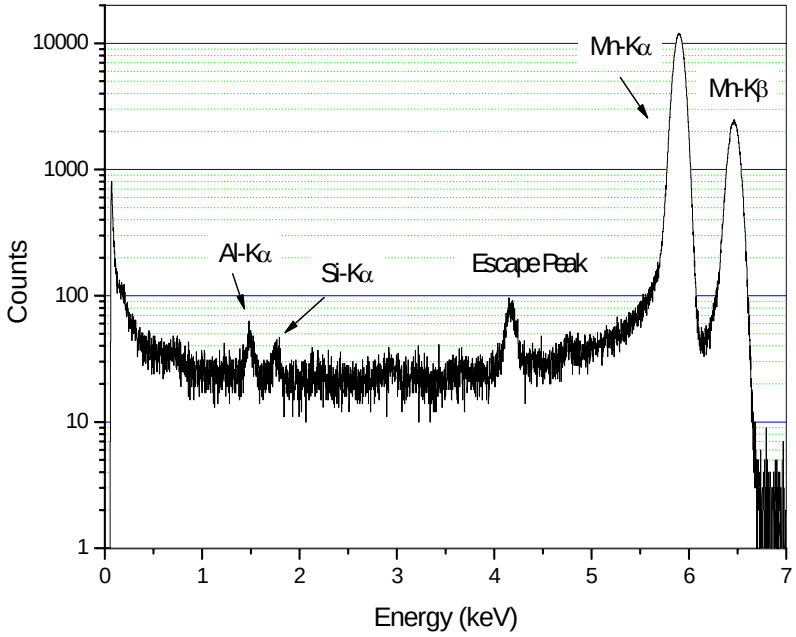
Processing thin detectors





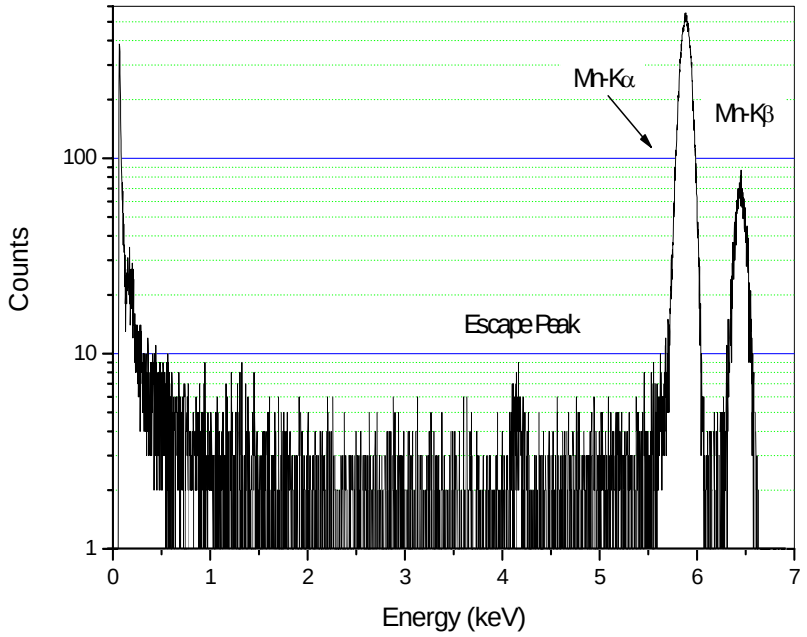


Energy resolution: best value



"Frontside" illumination:
Source illuminates electronic side

Energy resolution:
126 eV FWHM @ Mn-Ka Line
corresponding to 4.9 e^- ENC



"Backside" illumination:
Source on top of entrance window

Energy resolution:
132 eV FWHM @ Mn-Ka Line
corresponding to 6.6 e^- ENC

WFI requirements

Device dimensions

- Device active area 10.4 x 10.4 cm^2
- Monolithic sensor integrated onto a single wafer
- Device thickness 450 μm
- Pixel size 100 x 100 μm^2
- Total 1024 x 1024 pixel cells

Quantum efficiency

- Thin homogeneous entrance window
- Fill factor = 1
- QE @ C-Kα (282 eV) 90 %
- QE @ Si-Kα (1740 eV) 100 %
- QE @ Cu-Kα (8050 eV) 100 %
- QE @ 10 keV 96 %
- QE @ 20 keV 45 %

Spectroscopy

- Energy resolution @ Mn-Kα 125 eV
- Energy resolution @ C-Kα 50 eV
- System noise 3-5 e^- ENC

Readout timing

- Total readout time / frame 1 - 2 ms
- Processing time per detector row 2.5 - 4 μs
- Total raw data rate 2 GByte / s

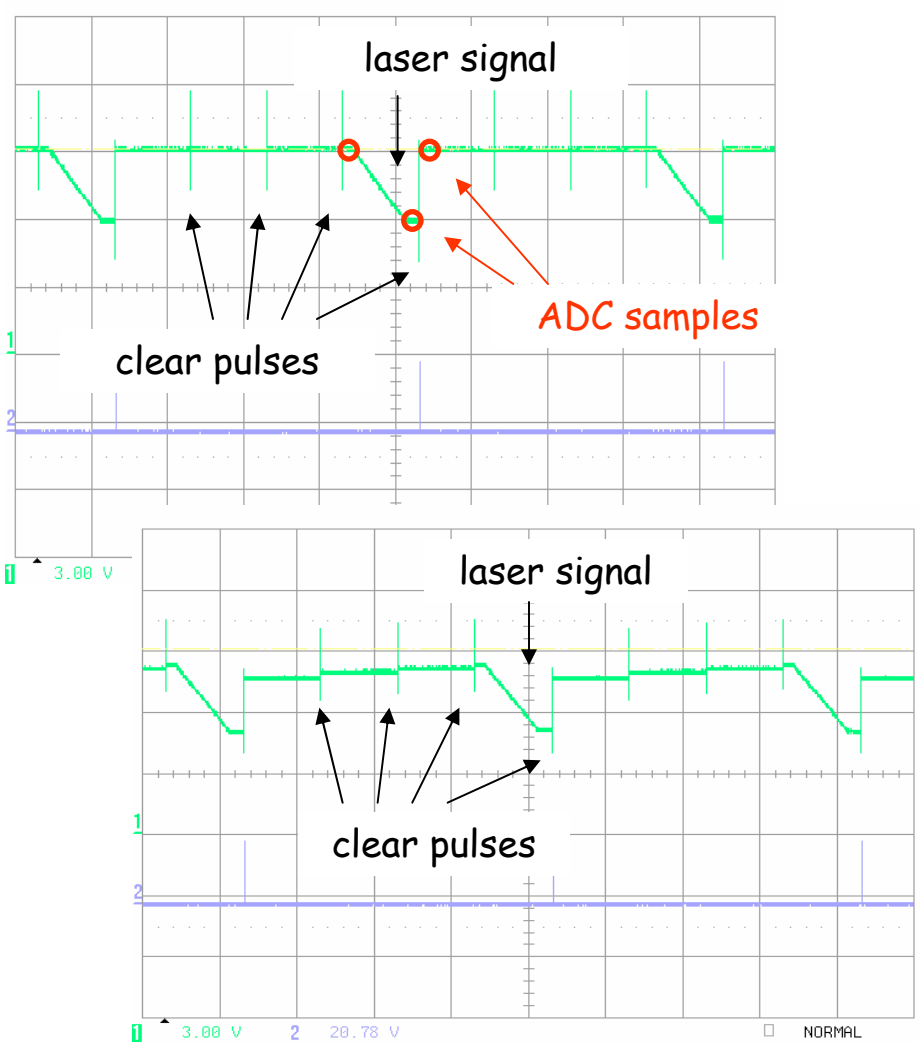
Measurement of clear efficiency

- Drain readout setup
- Clear pulse lengths > 150 ns feasible with setup
- Clear process by diffusion & drift
- Charge injection by laser in one cycle
- Number of dark cyles follow
- Observation of dc levels at pixel output
- Sampling before and after the laser signal and after the first clear

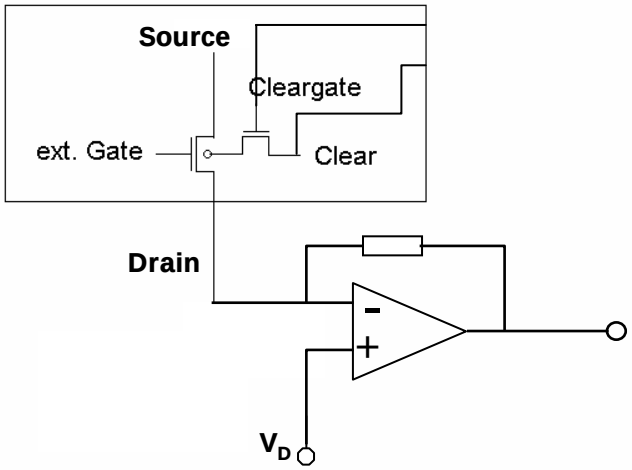
Case of incomplete clear:

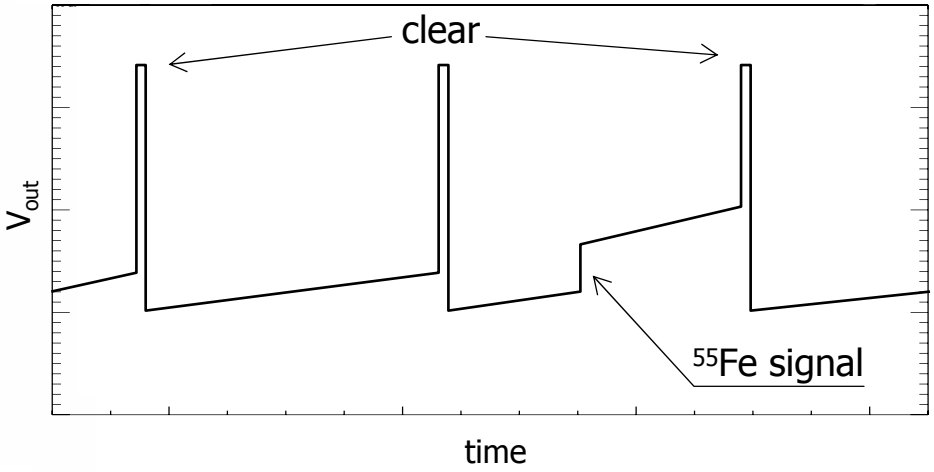
- Pixel in dynamic equilibrium
- Different dc levels after each clear
- No saturation of dc levels

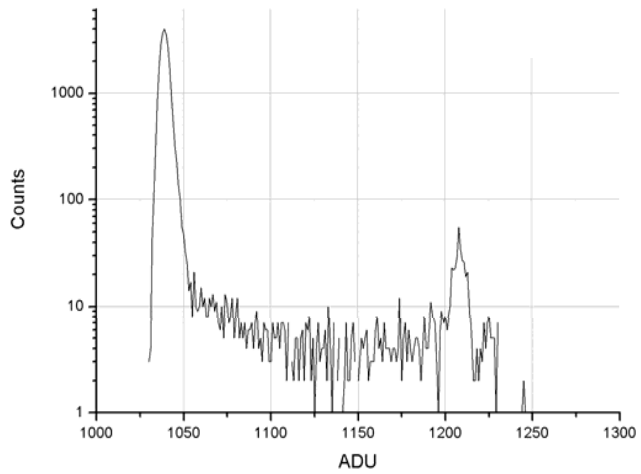
Result: Pulse height spectrum



Leakage current and g_q







non-irradiated:
Leakage current into the internal gate:

I_{Leak}=5 fA .. 22 fA

Internal amplification

g_q= 350 pA/e-

912 krad ^{60}Co:
Leakage current into the internal gate:

I_{Leak}=156 fA

Internal amplification

g_q= 335 pA/e-

Module Concept/Power Consumption

Total power consumption of the vtx-d in the active region (TDR design, 25 μm pixel)

DEPFET matrix only:

1st layer : 2 rows active, 30 μA · 5V · 650 · 2 · 8 = 1.6 W

2nd .. 5th layer: 1 row active, 30 μA · 5V · 1100 · 1 · 112 = 18.5 W

Steering chips: assuming 0.15 mW for an inactive, 300 mW for an active channel

1st layer : [(4998 · 0.15 mW)+(2 · 300mW)] · 8 = 10.8 W

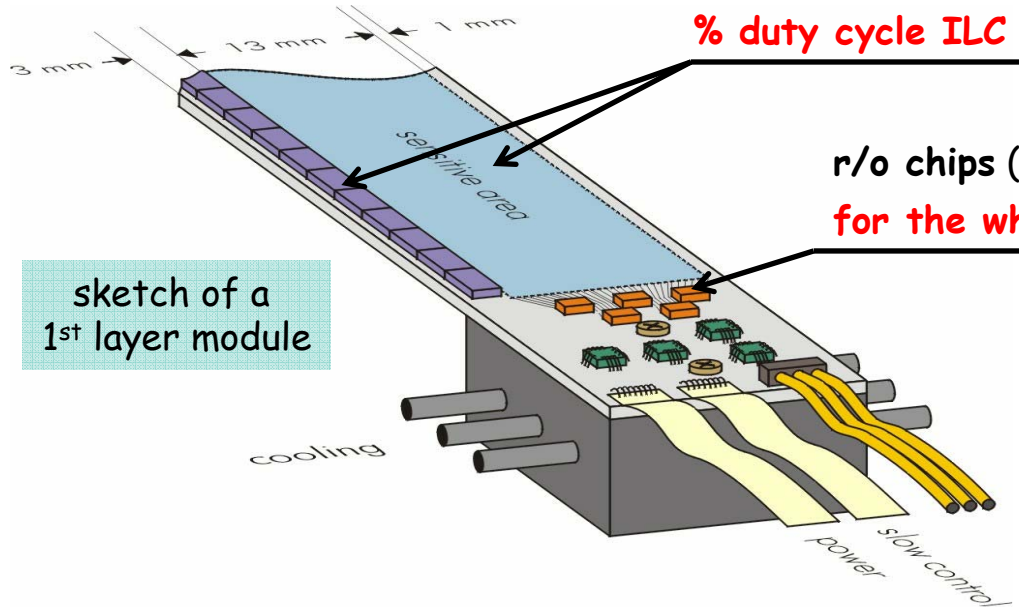
2nd ..5th layer: [(6249 · 0.15 mW)+(1 · 300mW)] · 112 = 138.6 W

Σ active region ≈ 170 W

% duty cycle ILC 1/200 → ≈ 0.9 W

r/o chips (current version):2.8 mW/chn.

for the whole vtx-d: ≈ 2W



sketch of a 1st layer module

Clear Gate after irradiation (^{60}Co)