First Results of
0.15μm CMOS SOI Pixel Detector

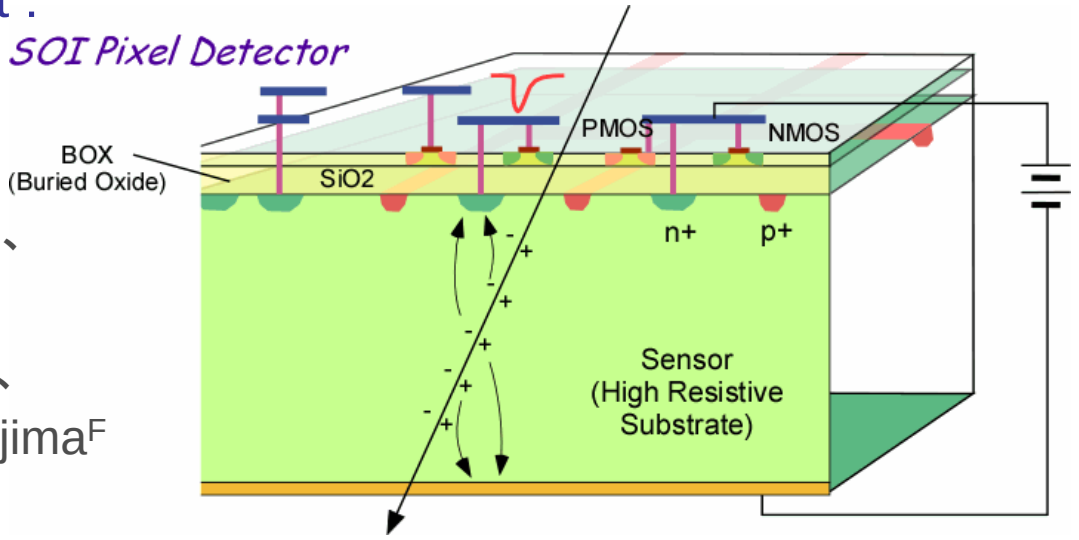
International Symposium on Detector Development
SLAC, CA, April 5, 2006

Yasuo Arai (KEK)

KEK Detector Technology Project :
[SOIPIX Group]

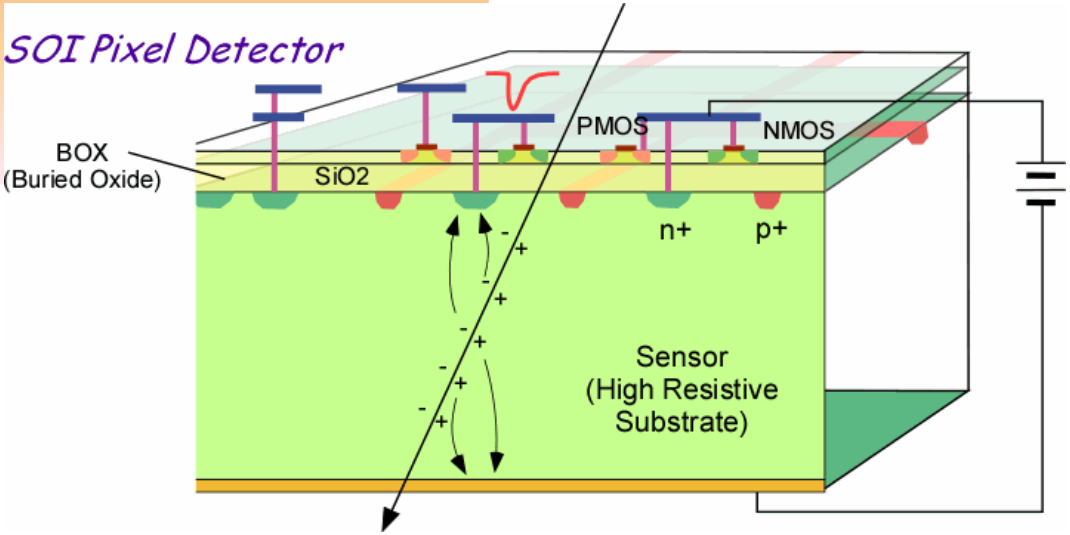
Y. Arai、Y. Ikegami、H. Ushiroda、
Y. Unno、O. Tajima、T. Tsuboyama、
S. Terada、M. Hazumi、H. Ikeda[A]、
K. Hara[B]、H. Ishino[C]、T. Kawasaki[D]、
Gary Varner[E], Elena Martin[E], Hiro Tajima[F]

KEK、JAXA[A]、U. Tsukuba[B]、TIT[C]、
Niigata U.[D]、U. Hawaii[E], SLAC[F]



OUTLINE

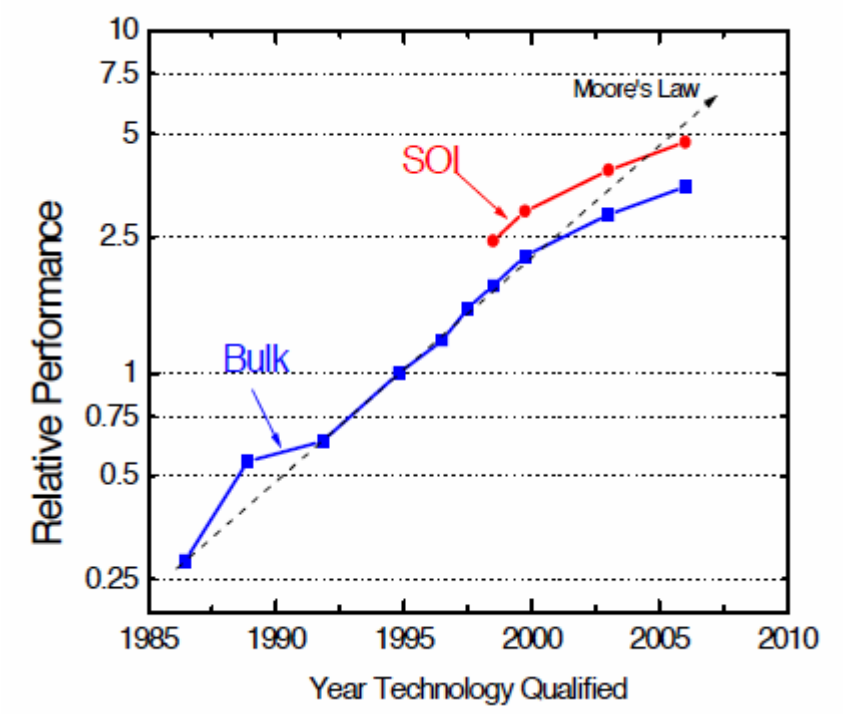
1. Introduction
   What is Silicon-On-Insulator?
2. SOI Pixel Development at KEK
3. Specific Issues on SOI Pixel
   TCAD Simulation
4. Test Results
5. Summary

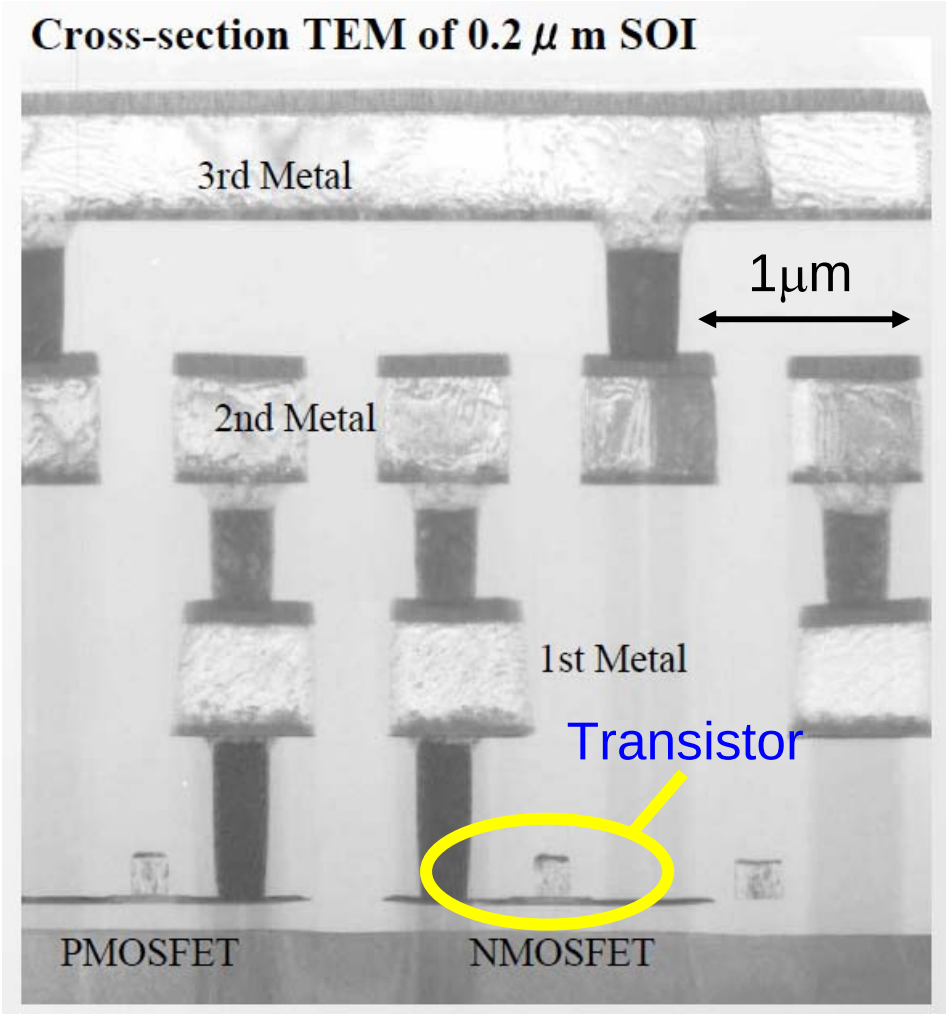


1. Introduction

What is Silicon-On-Insulator?

- A thin layer (50nm ~ 100μm) of Si layered on SiO_2
- Higher speed (up to 15%) and Lower power (up to 20%) over Bulk CMOS.



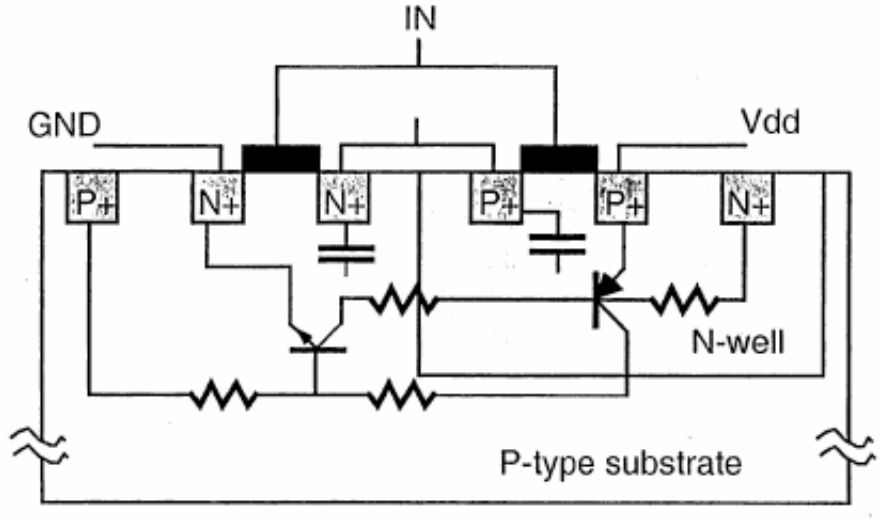


OKI Electric Industry Co., Ltd.

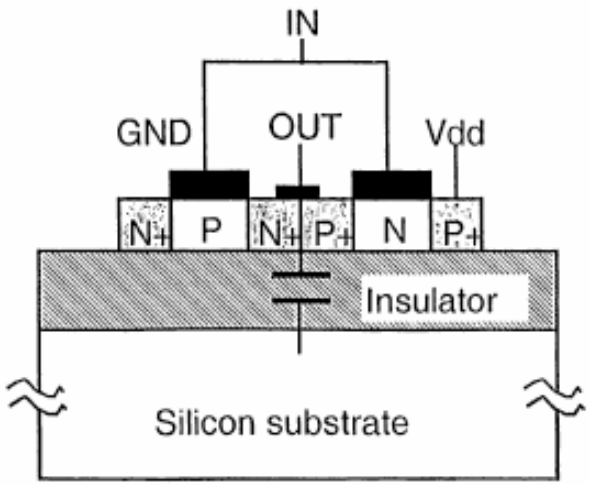
Feature of SOI-CMOS Devices

- Full Dielectric Isolation : *Latchup Free, Small Area*
- Low Junction Capacitance : *High Speed, Low Power*
- Low Leakage, Low Vth Shift : *High Temp. (~300 ºC) Application*
- High Soft Error Immunity : *Rad-Hard application*

Bulk CMOS



SOI CMOS

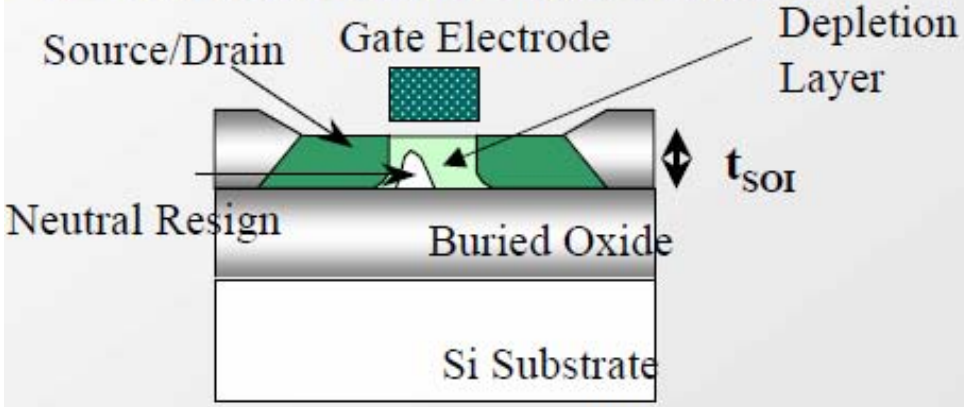


(Ref. 'SOI Technology' by Jean-Pierre Colinge, Springer)

PD vs. FD

PD-SOI (Partially Depleted)

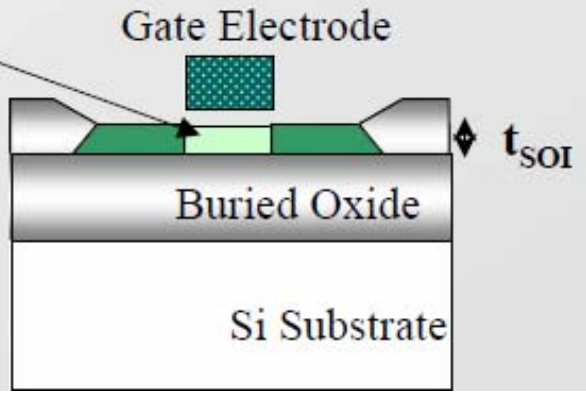
- ◆Thick SOI Thickness (T_{SOI}) ~0.1- 0.2μm
- ◆Depletion Layer < T_{SOI}
- ◇Large Floating body effect
- ◇High Drive Current by Kink effect
  - → High speed application
- ◇Compatible Process with Bulk-Si



IBM PowerPC, AMD Athlon, Sony Cell …

FD-SOI (Fully Depleted)

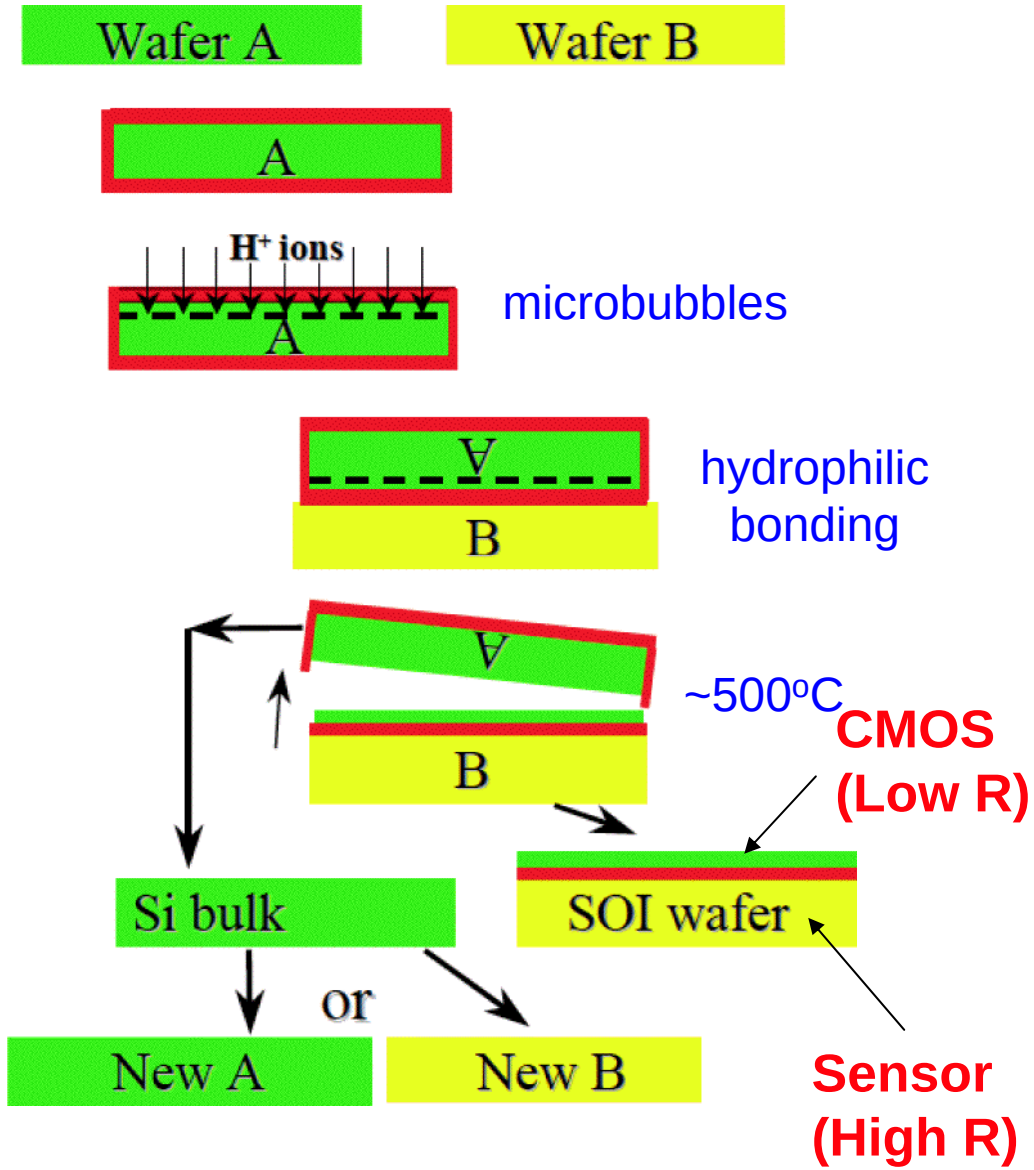
- ◆Thin SOI Thickness (T_{SOI}) < 0.05μm
- ◆ Depletion Layer > T_{SOI}
- ◇Less Floating body effect
- ◇Better Subthreshold Slopes
  - → Low-V_{th} is available
- ◇Process Issues in thin-film SOI



OKI Radio Controlled Wrist Watch (CASIO)

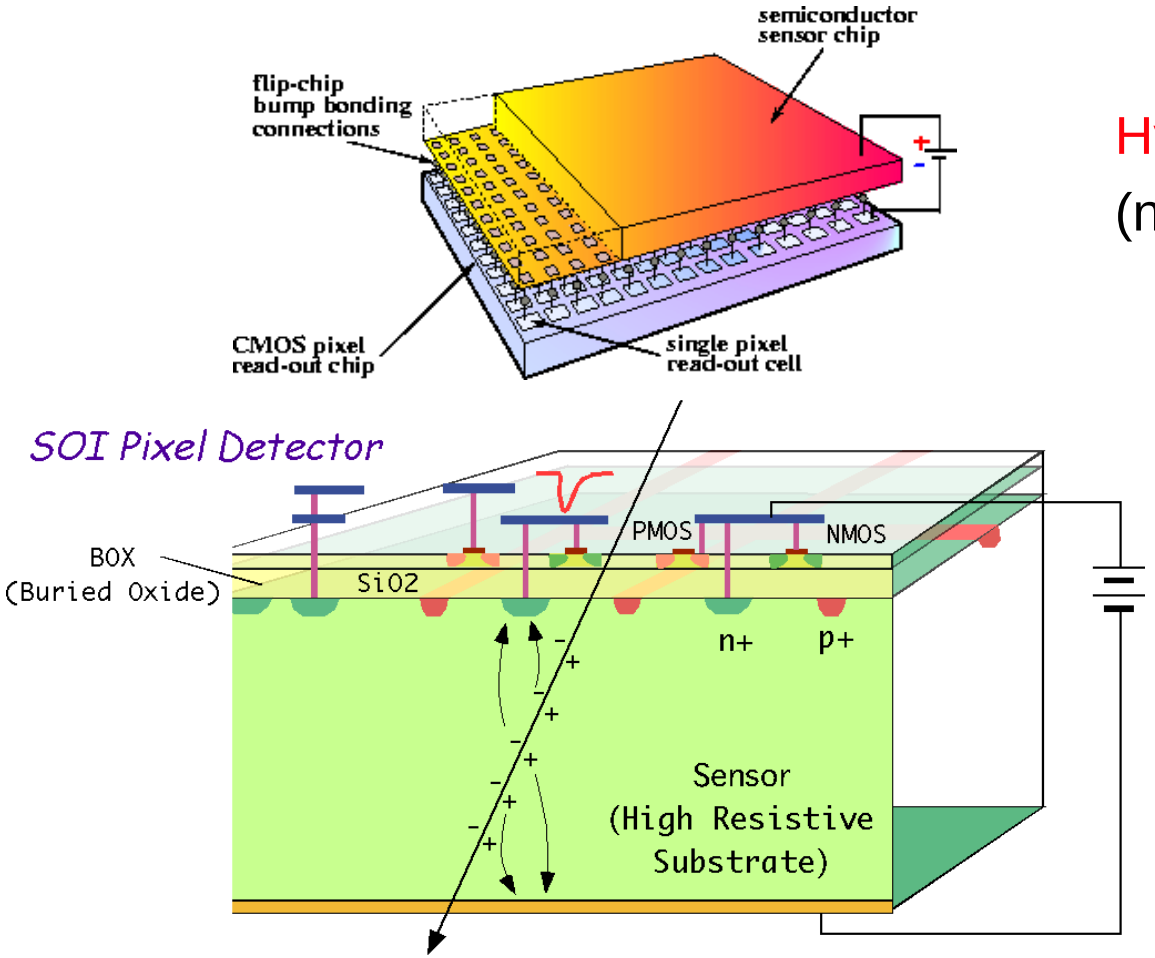
SOI Wafer Fabrication（UNIBOND™, SOITEC）

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B



2. SOI Pixel Development at KEK

Last spring, New Detector R&D projects were called at KEK, and we proposed Development of SOI (Silicon-On-Insulator) *Pixel Detector. Main members consist of Belle and ATLAS silicon detector group.*



Hybrid Pixel Detector

(need many bump bondings)

SOI Pixel Detector

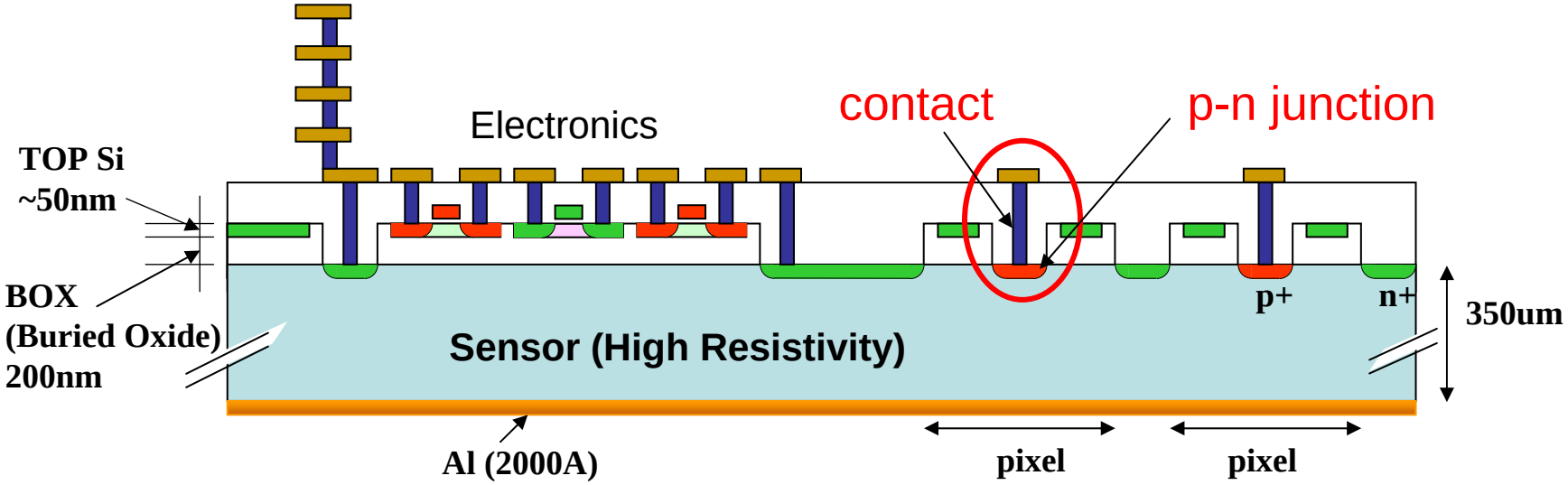
Monolithic Detector with Sensor(Hi-R) and Electronics(Low-R)

Feature of Our SOI Pixel Detector

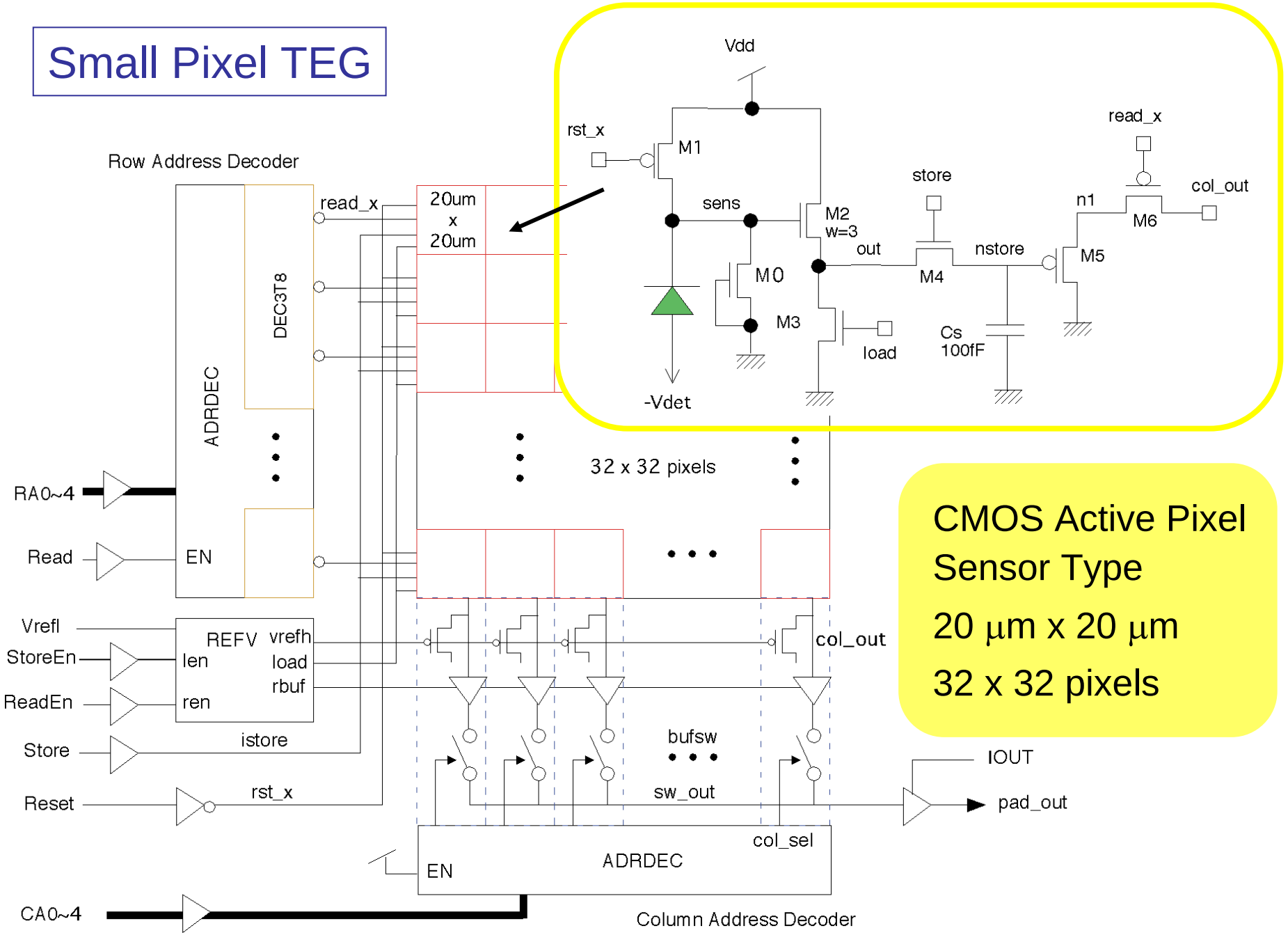
- Using Commercial 0.15μm FD-SOI process (OKI Elec. Ind.).
- SOI Wafer (SOITEC Hi-R, 150 mmϕ)
  Top Si : Cz, ~18 Ω-cm, p-type, 50 nm thick
  Buried Oxide: 200 nm thick
  Handle wafer: Cz、Hi-R >1k Ω-cm (*No type assignment by supplier)*, 650 μm thick (thinned after process <350μm)
- Multi Project Wafer (Masks are shared with other design) + additional process step.
- Add only 3 mask layers to create sensor (p+, n+, and contact to substrate).
- Back side is plated with Al (200 nm).

History

- ’05. 6: OKI agreed on SOIPIX development with us.
- ’05.10: 3 x 2（for p/n substrate) + 3 chips (total 9 chips) submitted.
  （32x32 small pixel, 4x4 large pixel, Short strip, Tr TEG ...)
- ’05.12: Test of contact fabrication.
- ’06. 2: Test of p-n junction fabrication.
- ’06.3 middle : Process ends.
- ’06.3.30 Bare Chip Delivered. (-> so the results are very preliminary)



Small Pixel TEG



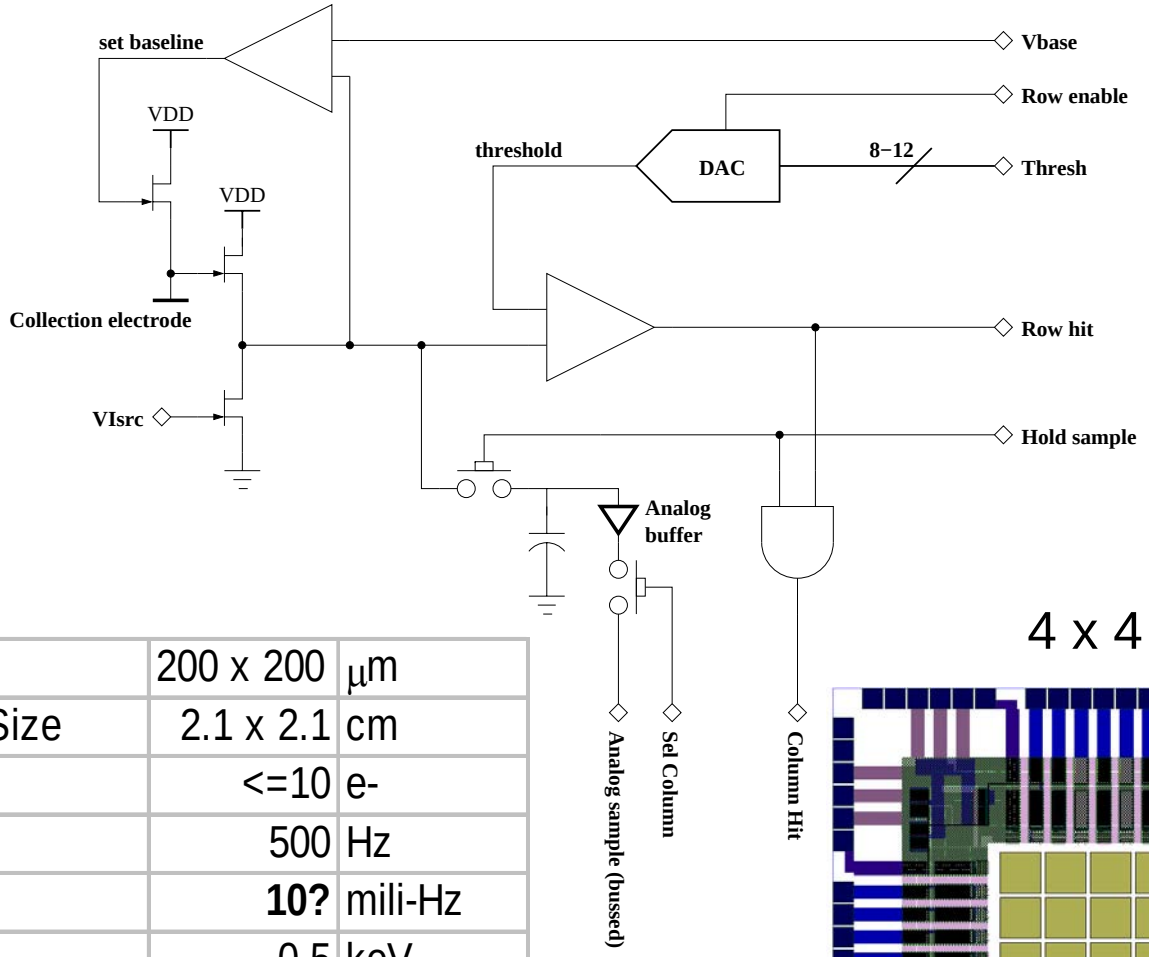
CMOS Active Pixel Sensor Type

20 μm x 20 μm

32 x 32 pixels

IHXCP (Imaging Hard X-Ray Compton Polarimeter) TEG

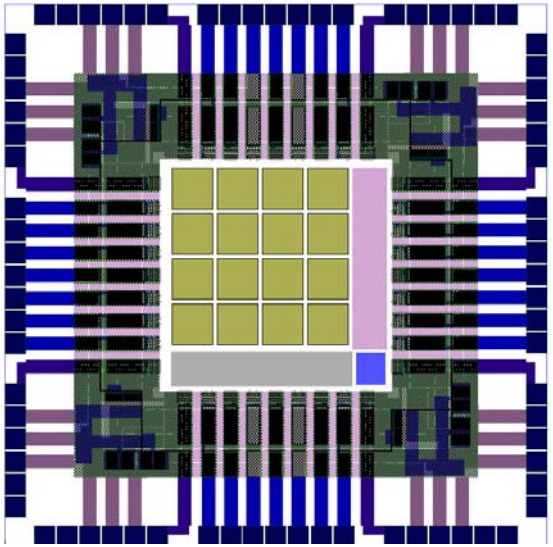
U of Hawaii &
SLAC



Target Specification

Pixel Size	200 x 200	μm
Pixel Array (Detector) Size	2.1 x 2.1	cm
Noise	<=10	e-
Global Trigger Rate	500	Hz
Single Pixel Rate	**10?**	mili-Hz
Trigger Threshold	0.5	keV
Trigger Latency	1-2	μs
Power	200	μW/pixel
ADC precision	12	bits

4 x 4 pixels



3. Specific Issues on SOI Pixel

- **n+, p+ implant**

  → Formed with Tr Source/Drain not to increase number of masks.

- **Thinning**

  → Wafer is thinned from 650um to 350um. Further thinning is possible.

- **Back Side process**

  → No implant on back side. Just add Al (2000 A) Plating.

- **Thermal Donor generation**

  Type of the high-R wafer may change by TD generation during process.

  → We prepared both p & n substrate designs.

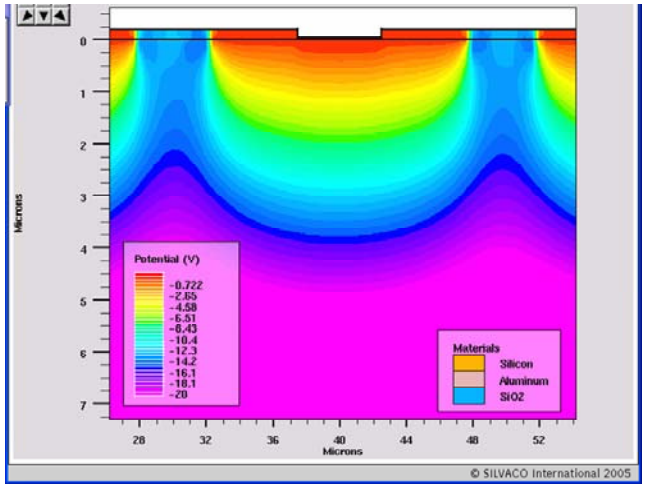
- **Back Gate Effect to SOI Tr**

  Substrate works as back gate, so the voltage must be low under Tr.

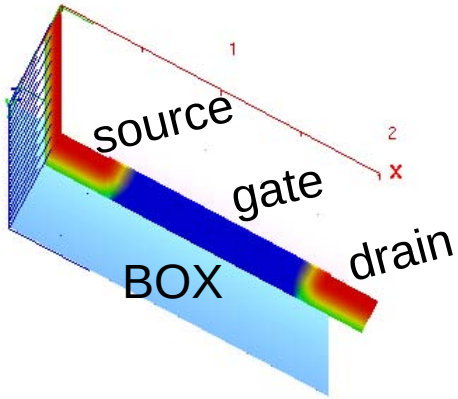
  → All Tr are placed within Guard Ring, and body is tied to VDD/VSS.

3D Process/Device Simulator ENEXSS

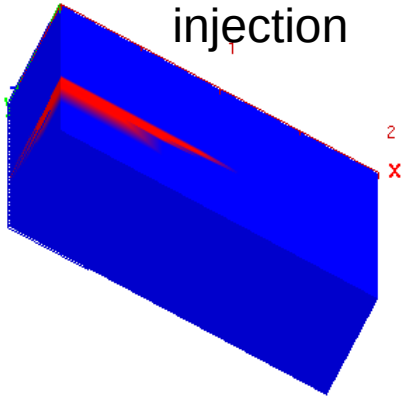
- Developed by SELETE (Japan Consortium) (http://www.selete.co.jp/)
- Full 3D simulation

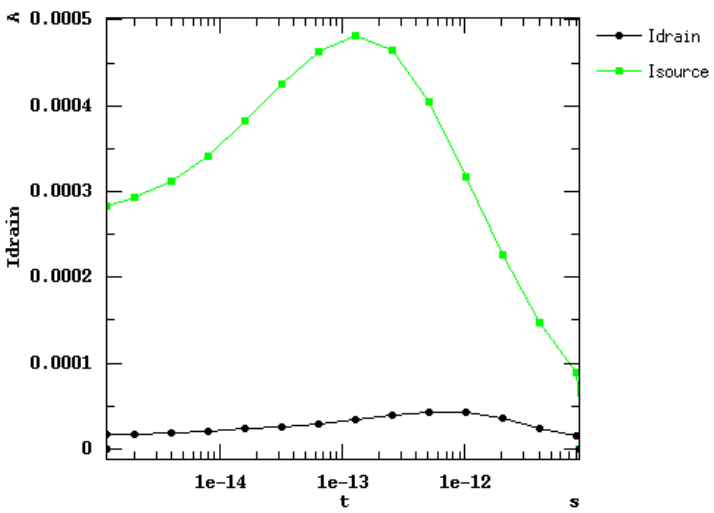


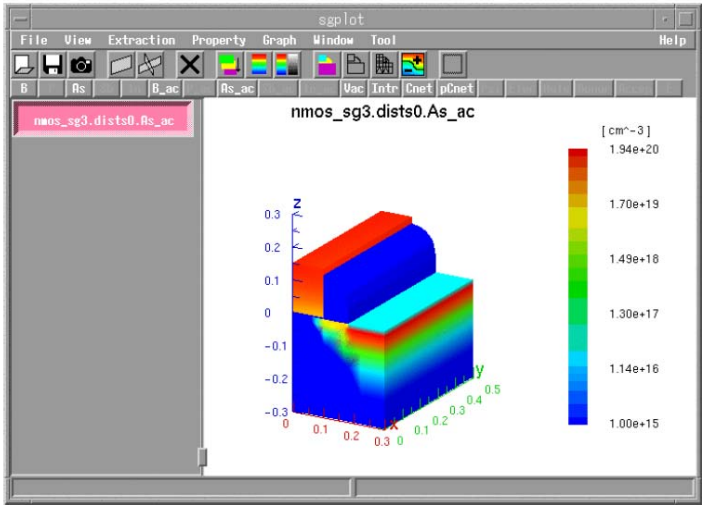
SOI NMOS



α particle injection





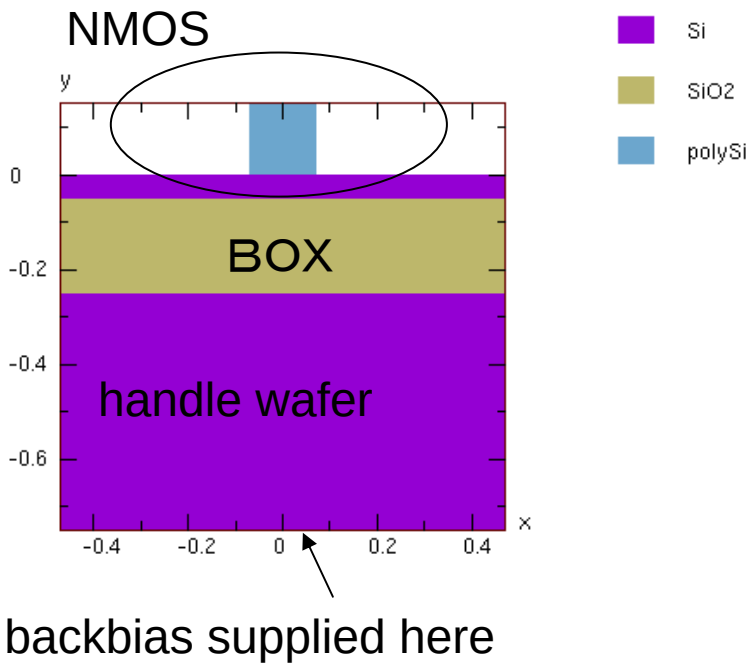


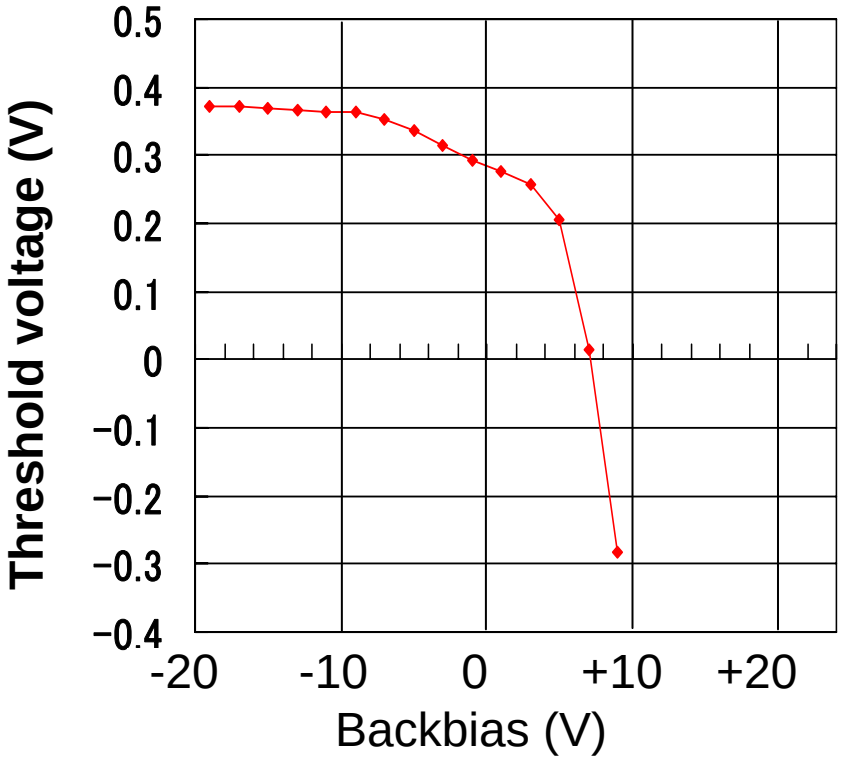
Useful to get

- Field Map
- Device Characteristics
- Signal generated by particle, etc.

Back Bias Simulation

TCAD: ENEXSS

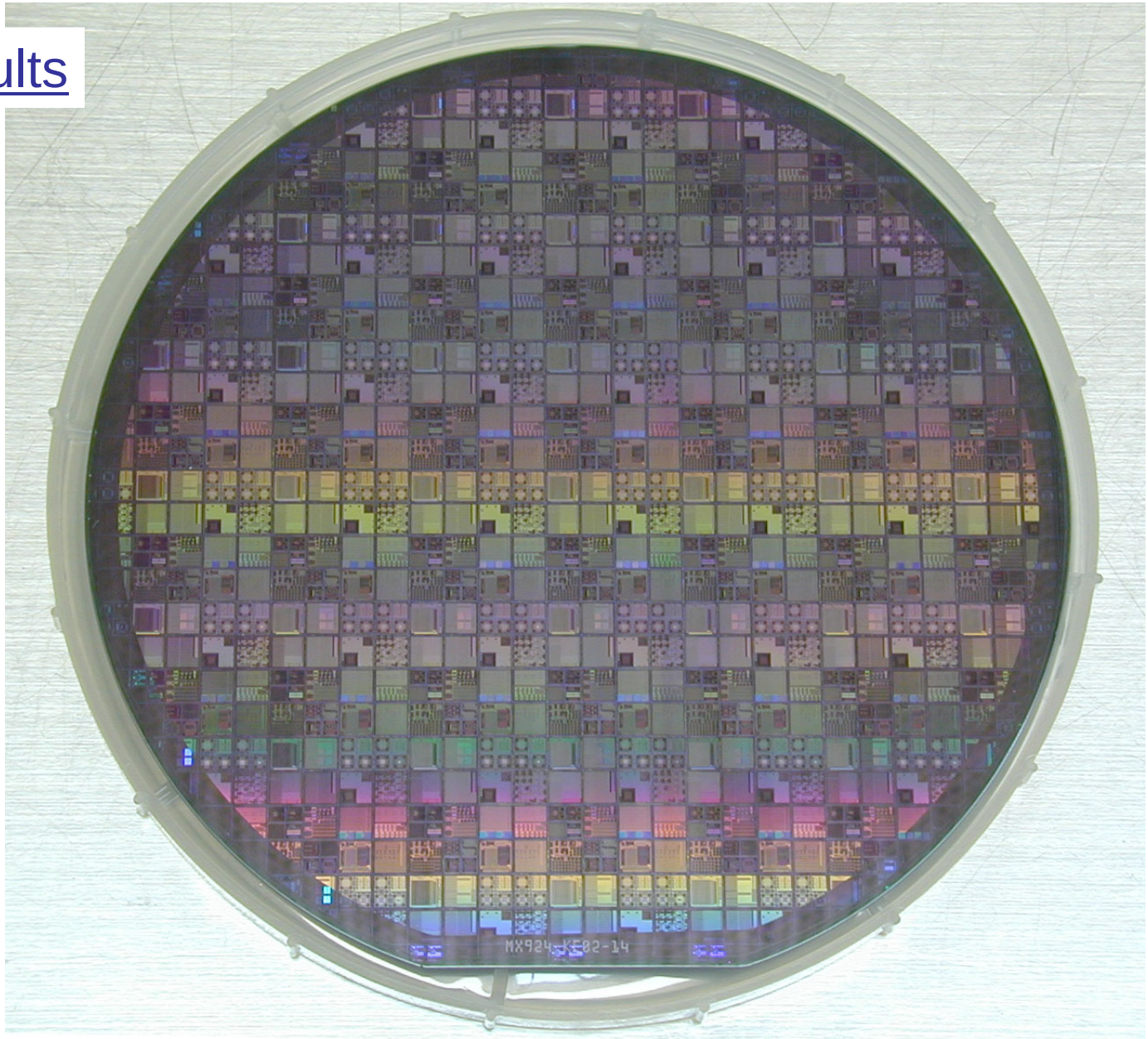




With |back bias| > 8V, NMOS or PMOS become always ON.

Voltage of substrate under Tr must be kept low.

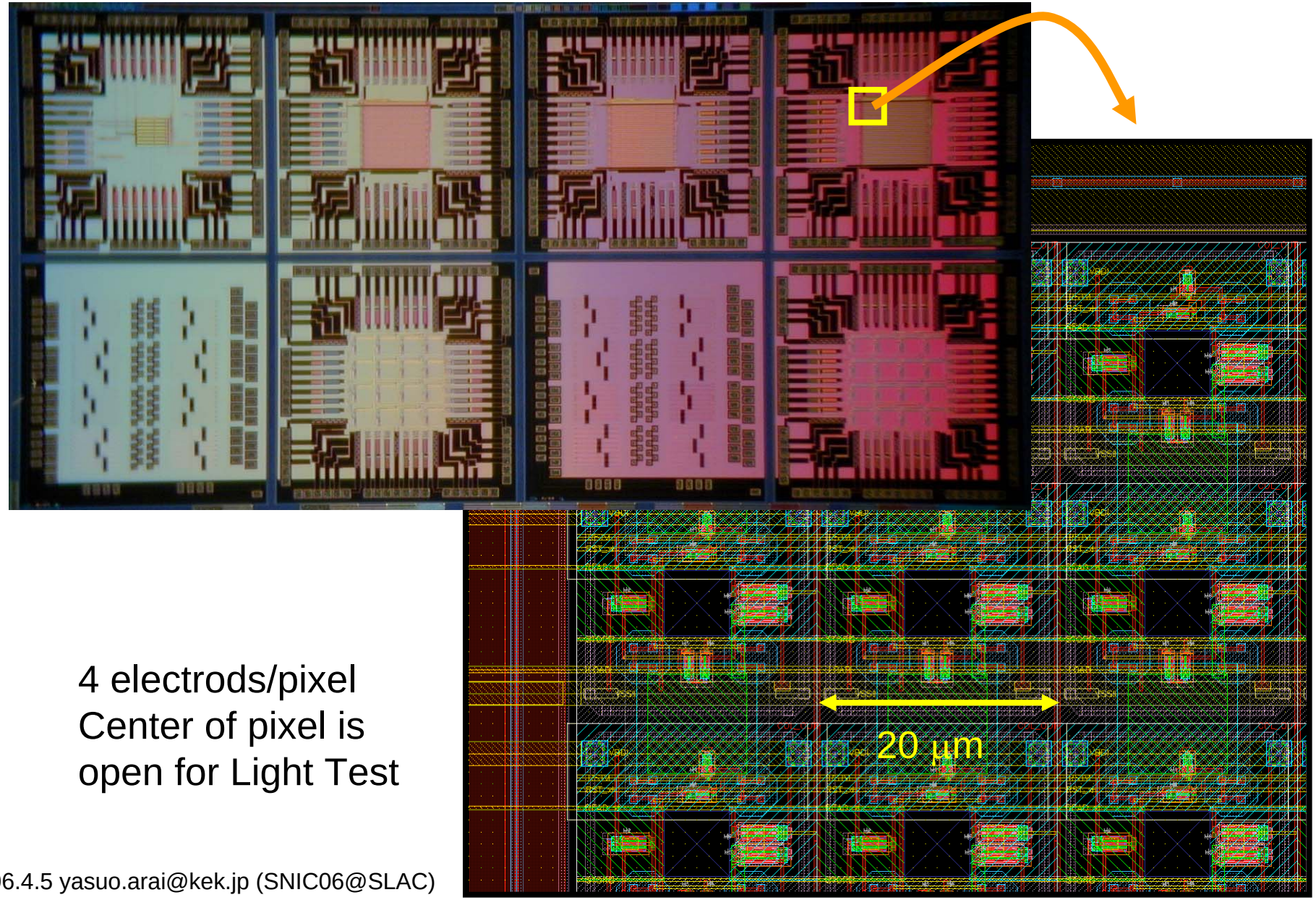
4. Test Results



MPW Wafer
150 mmϕ

TEG Chip Layout

← 2.5 mm →

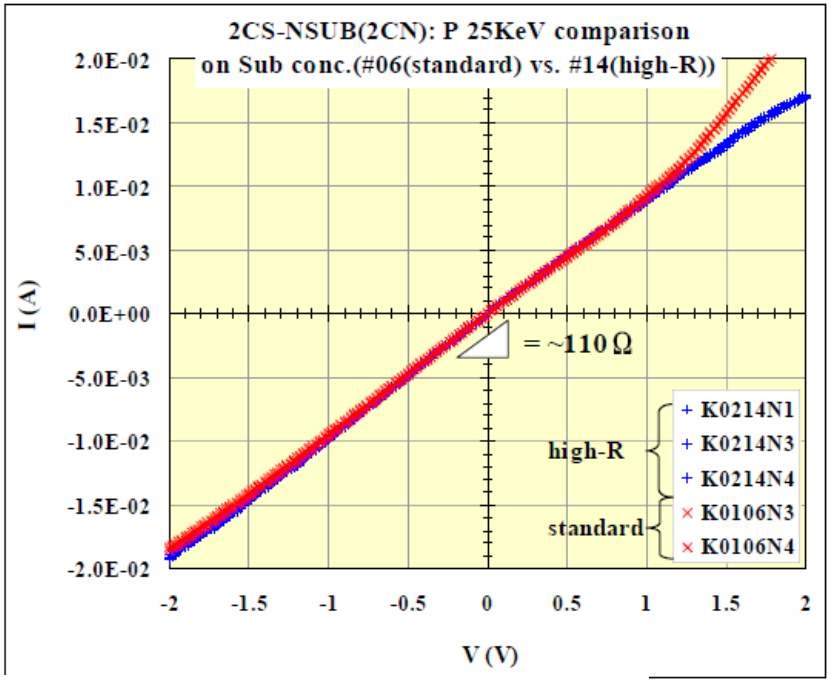


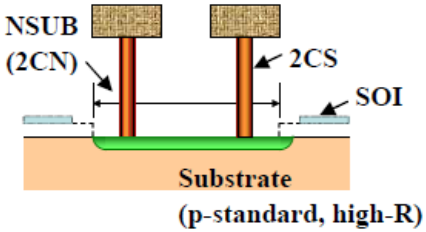
4 electrods/pixel
Center of pixel is
open for Light Test

2006.4.5 yasuo.arai@kek.jp (SNIC06@SLAC)

Contact & Sheet Resistance

n+ contact

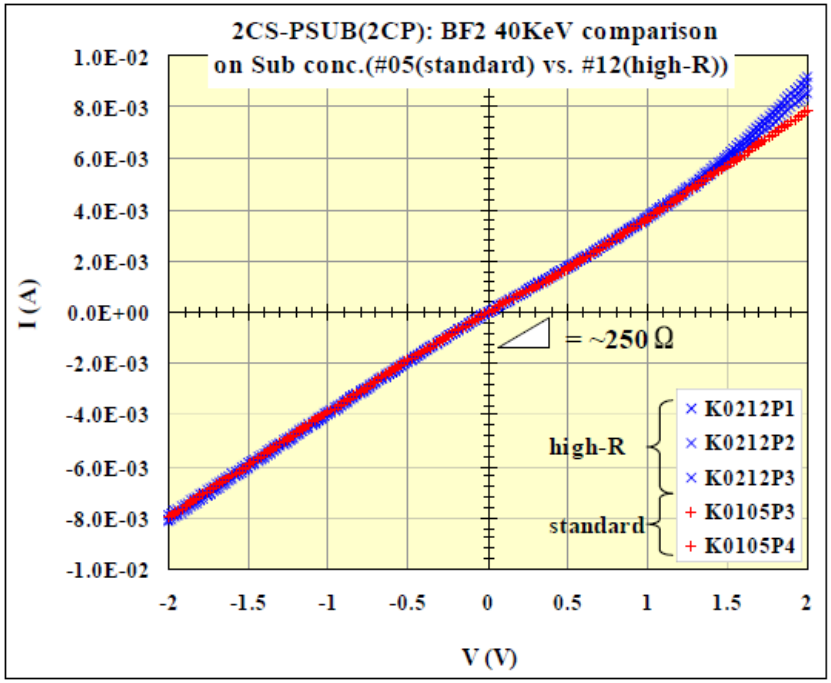


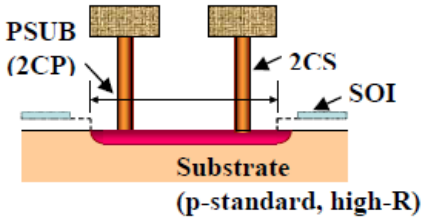


Hi-R (> 1k Ωcm)

Std. wafer
(p+, ~13 Ωcm)

p+ contact





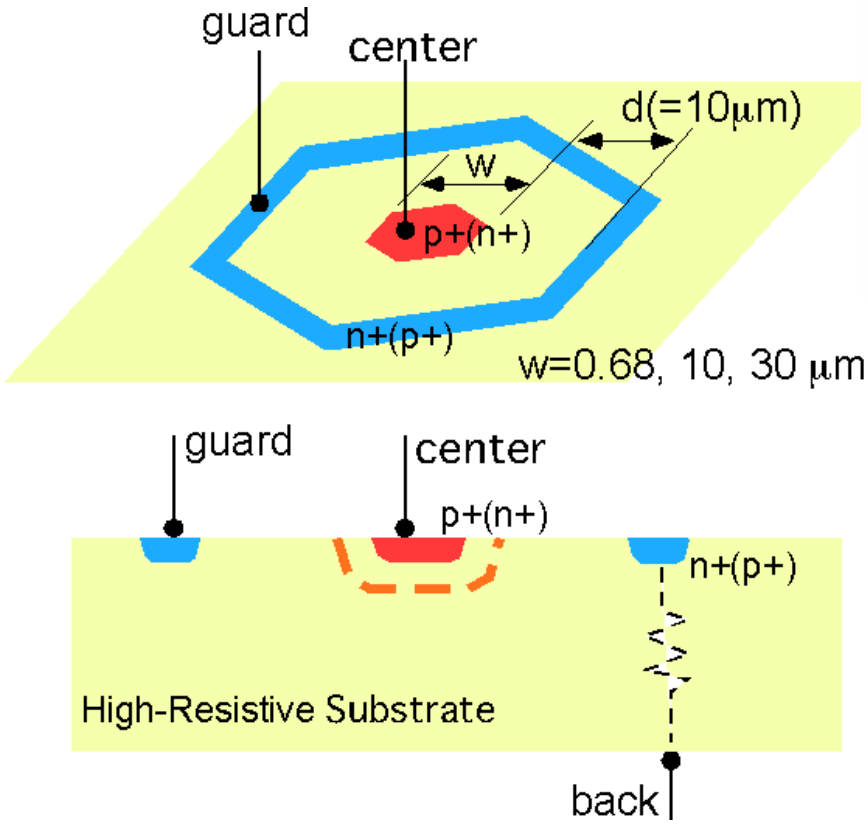
Hi-R (> 1k Ωcm)

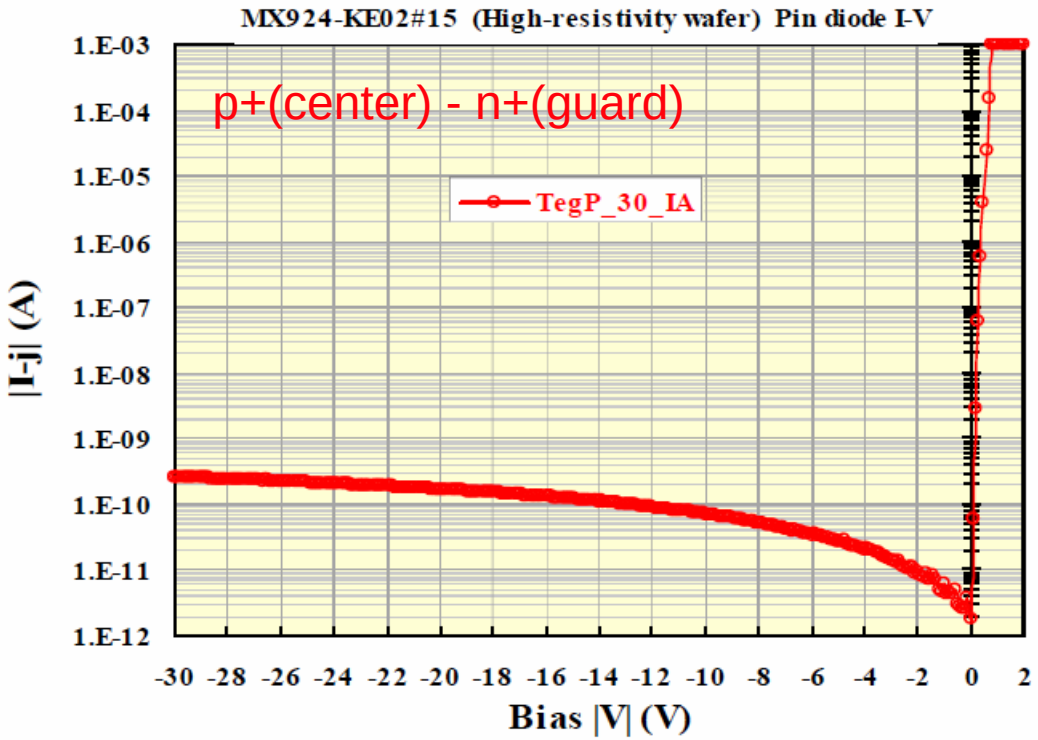
Std. wafer
(p+, ~13 Ωcm)

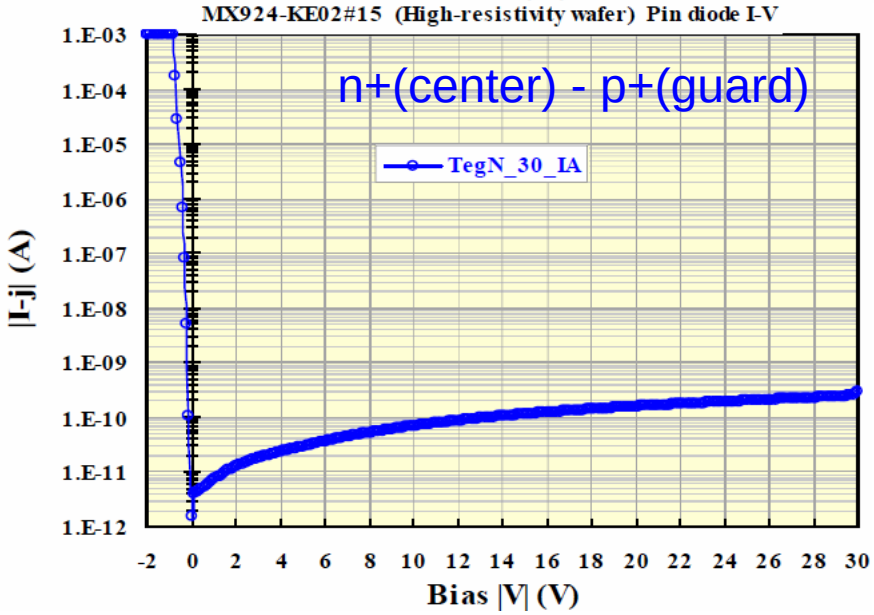
[Sheet R]
n+ : 33 Ω/square
p+ : 136 Ω/square
[Contact]
(0.16x0.16um^2)
n+ : 87 Ω
p+ : 218 Ω

p-n junction
I-V characteristics

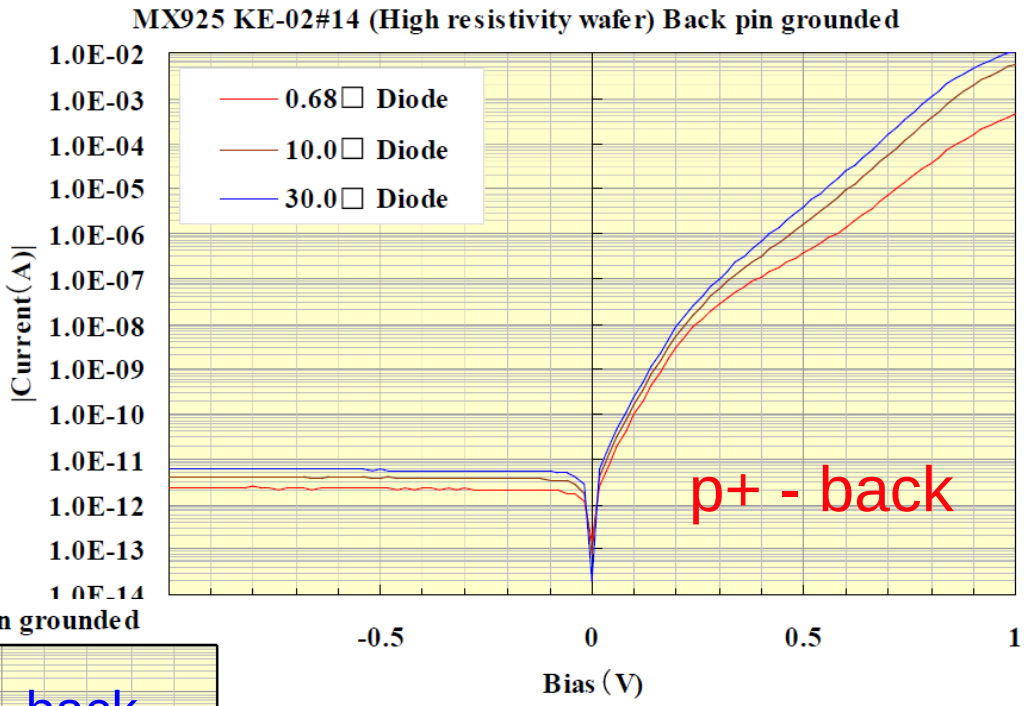
p+(center) - n+ (guard) &
n+(center) - p+(guard)

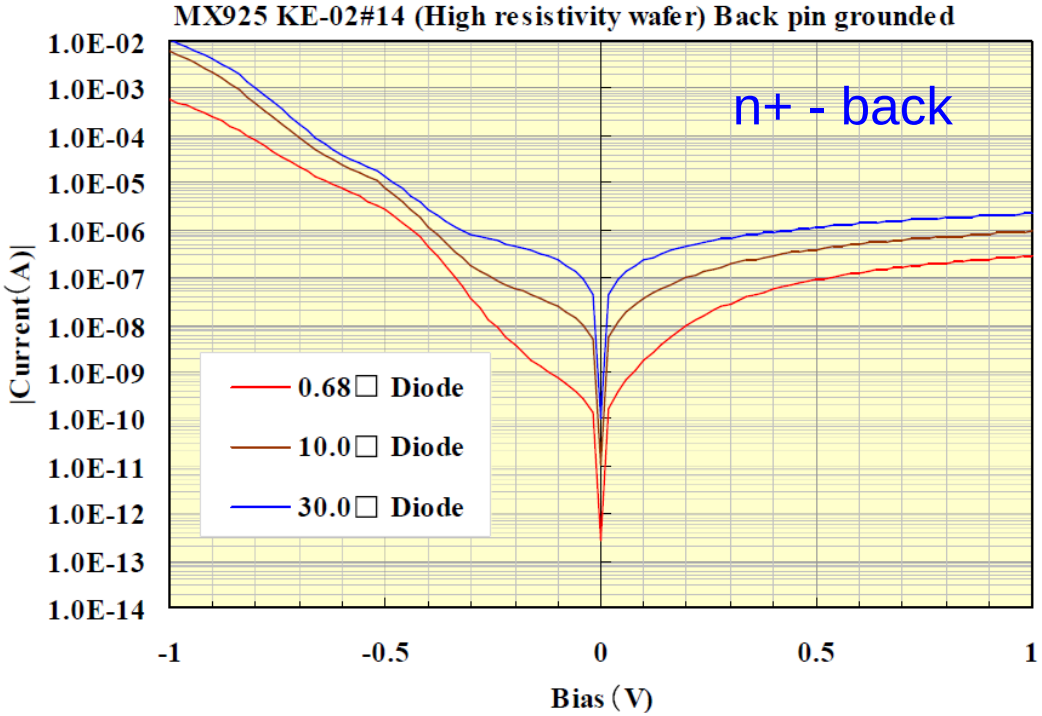






n+ / p+ --- back
I-V characteristics





n+(center) – back is Ohmic
→ Substrate is n-type

Substrate Resistivity

Very Preliminary!

[before process]

No type assign, > 1 kΩcm

[after process] (4-points measurement)

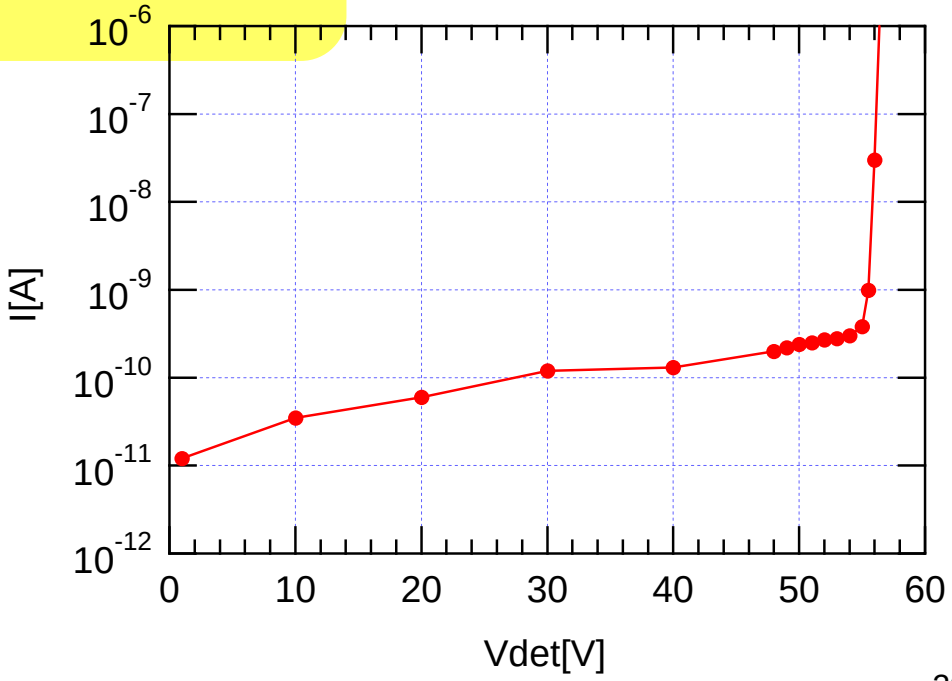
n-type, ρ ~700 Ωcm (->N_B~6x10^{12} cm^{-3})

I-V Characteristic

10um x 460um strip

I < 1nA @Vdet = 56 V

Depletion ~ 100 μm ?



5. Summary

- We have started development of Monolithic SOI Pixel Detector.
- The detector has sensor in high-resistive Si and CMOS circuit in low-resistive Si.
- We are using commercial (OKI 0.15 μm SOI) process with commercial wafer (SOITEC Hi-R) with only adding 3 masks.
- 3-D TCAD simulations for sensor/device study are being done with ENEXSS。
- Good substrate contact and p-n junction are confirmed with the first run wafer.
- We found type of handle wafer is ‘n’, and have enough resistivity.
- 9 kinds of TEG chips are received at the end of March, and showing promising results. Detailed tests will be done soon.
- We would like to apply this technique to Super-B, SLHC, ILC and X-ray detectors.