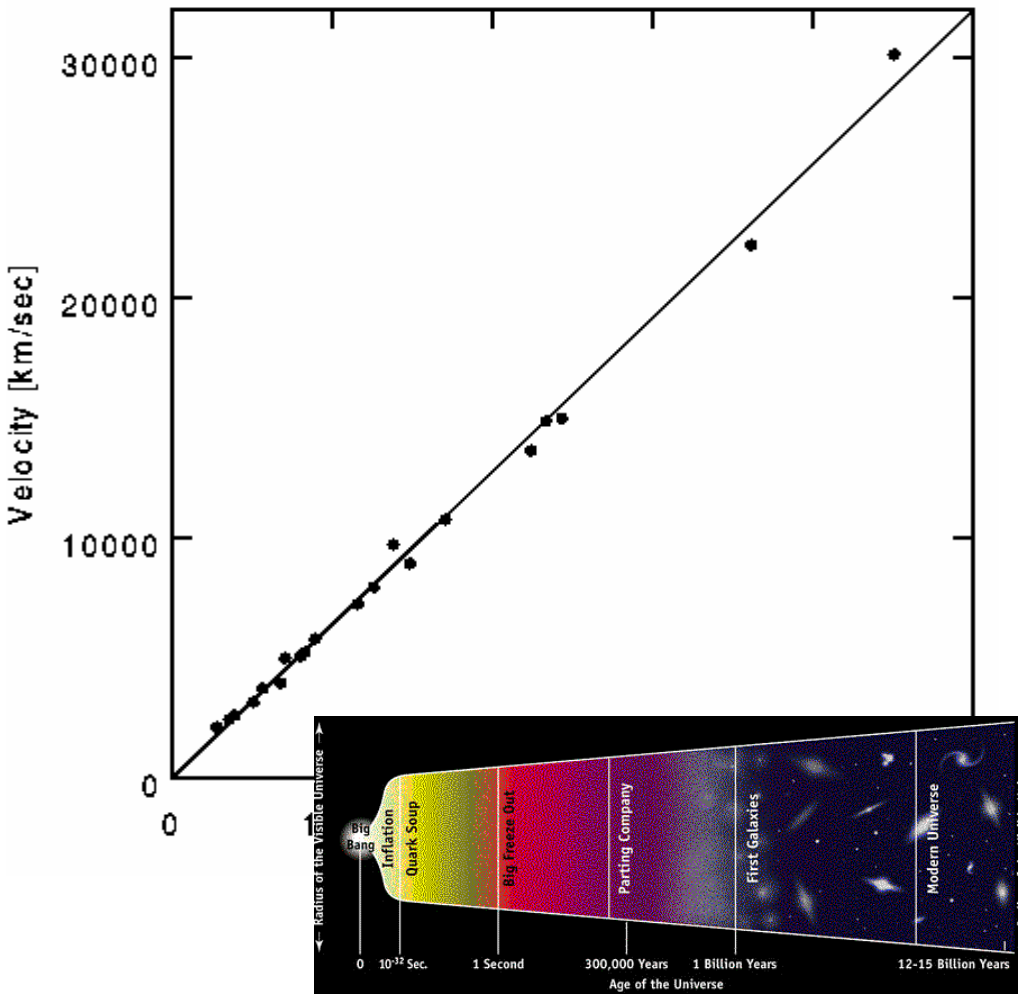
Future Trends in Microelectronics – Impact on Detector Readout

Paul O'Connor

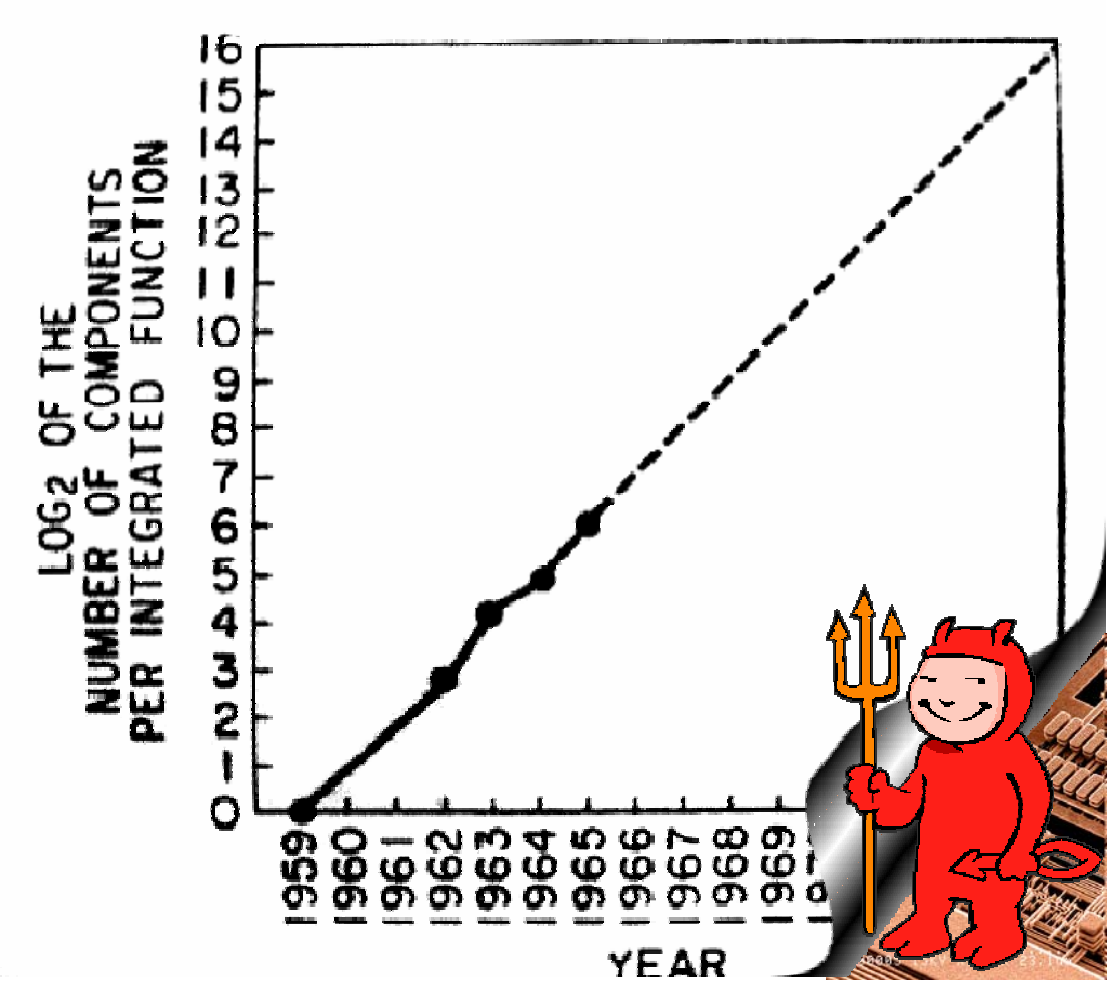
Outline

- CMOS Technology Scaling
- Analog Circuits
- Radiation Effects
- Cost

Edwin Hubble

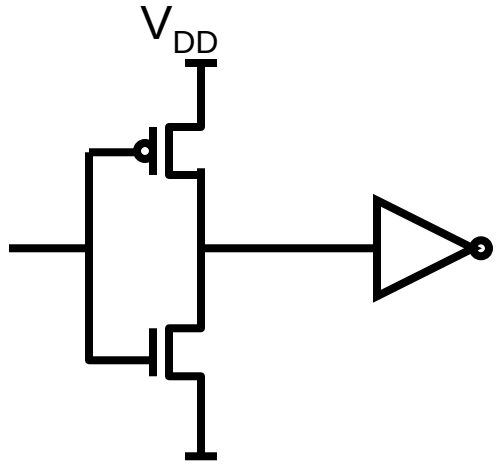


Gordon Moore

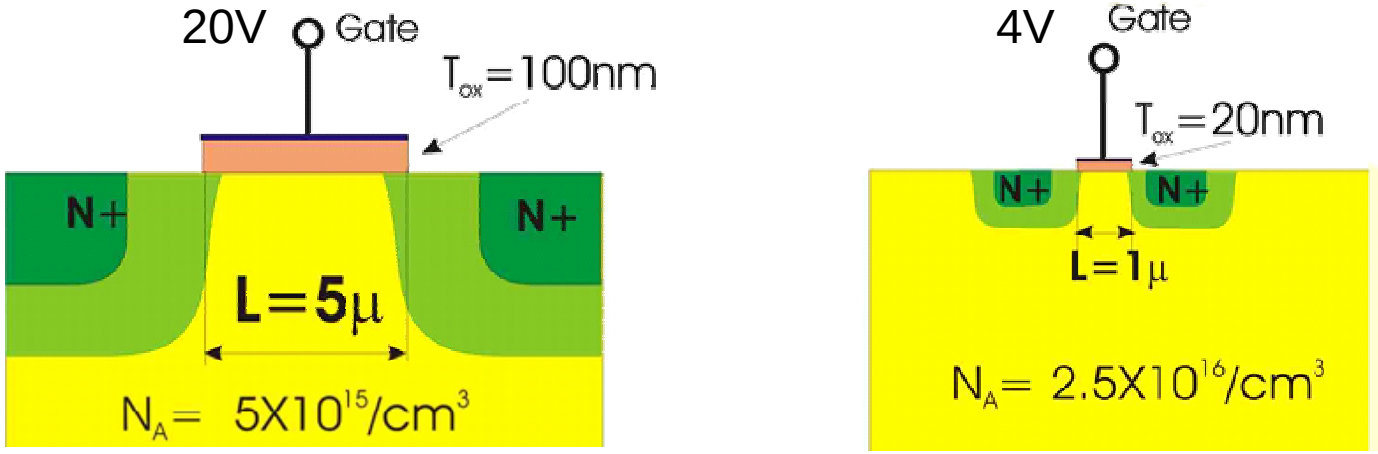


CMOS Logic Element

- Pair of nearly-ideal switches in series
- Complementary polarity $\Rightarrow$ common control voltage
- input impedance ~ ∞
- V_{DD}-tolerant
- Zero static power



MOSFET Scaling



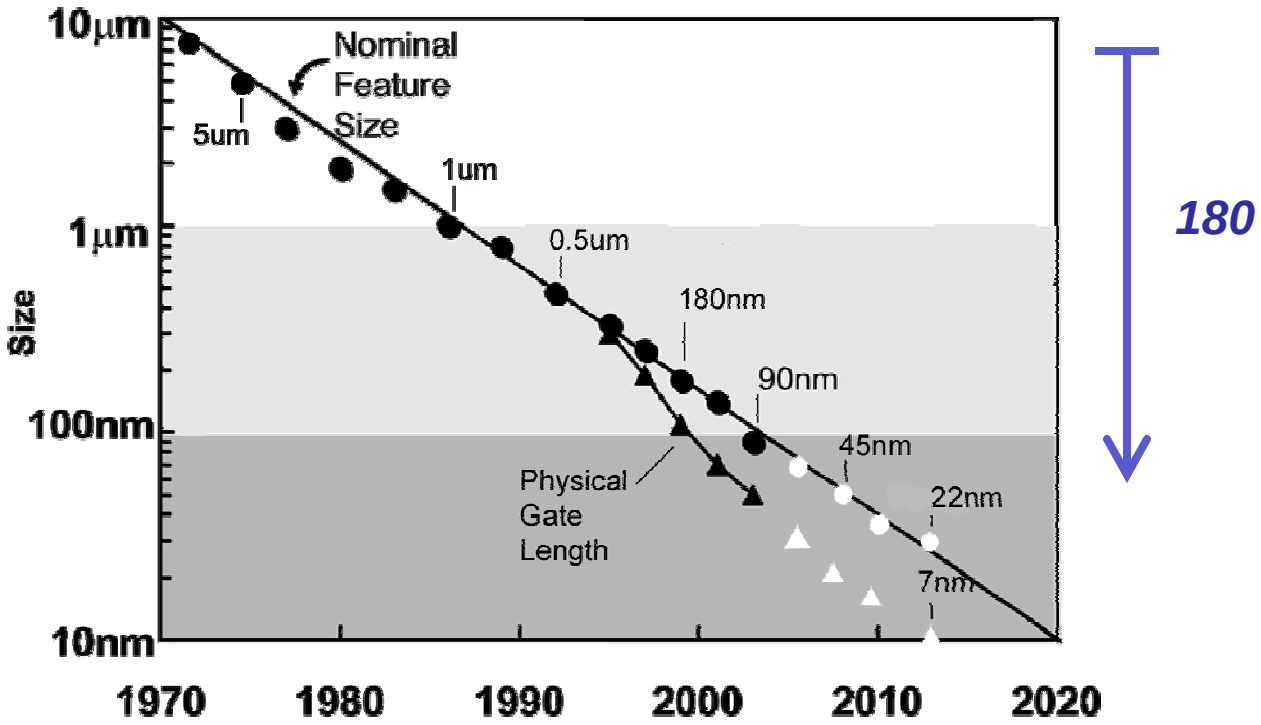
- Voltages, dimensions reduced by α
- Results:

$\vec{E}$ =		const.
Conductance	I/V	const.
Capacitance		$\frac{1}{\alpha}$
Speed	I/CV	α

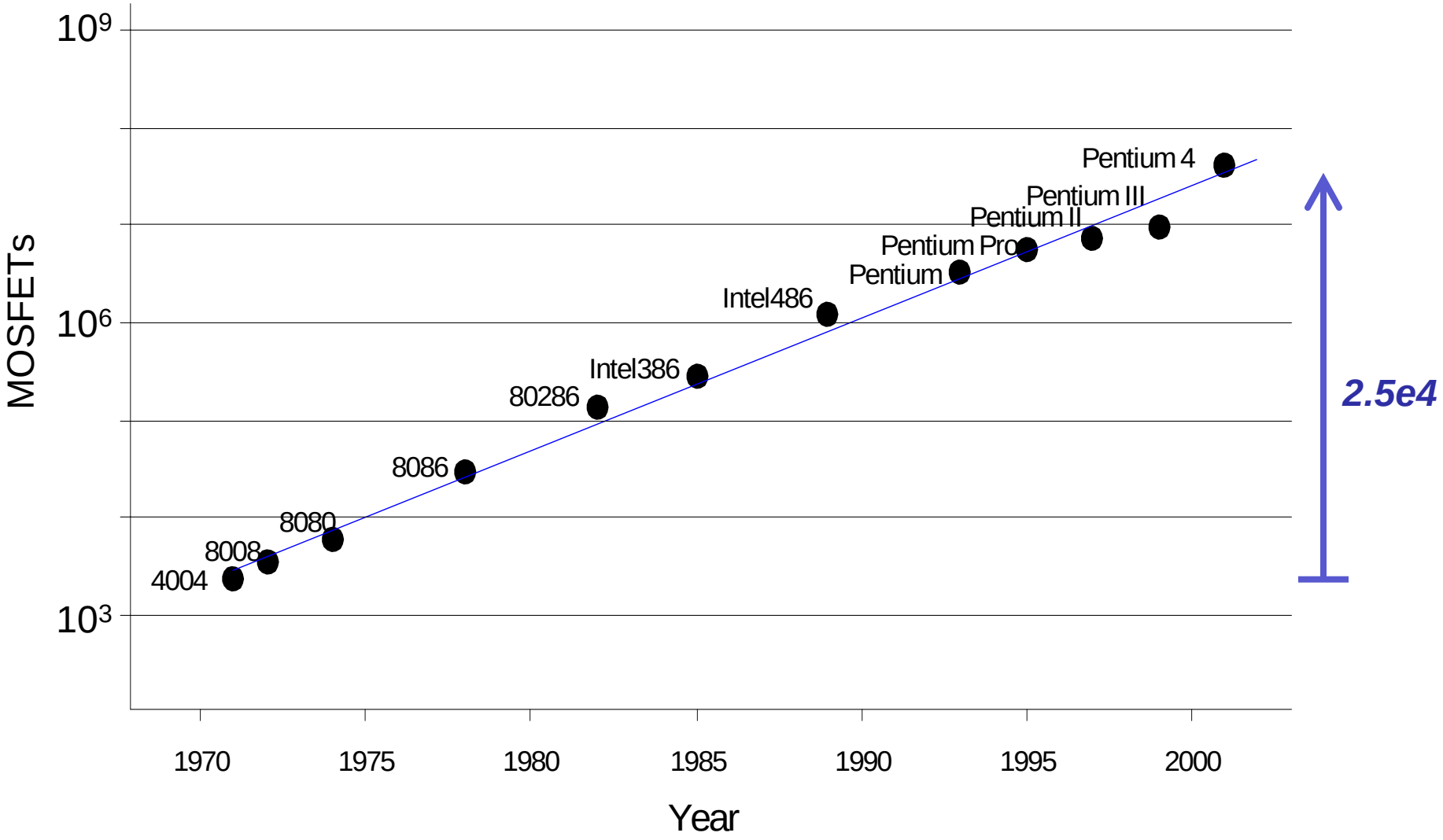
Switching energy	CV^2	$\frac{1}{\alpha^3}$
Power/gate	$CV^2 f$	$\frac{1}{\alpha^2}$
Density		α^2
Power density		const.

Industry Scaling Roadmap

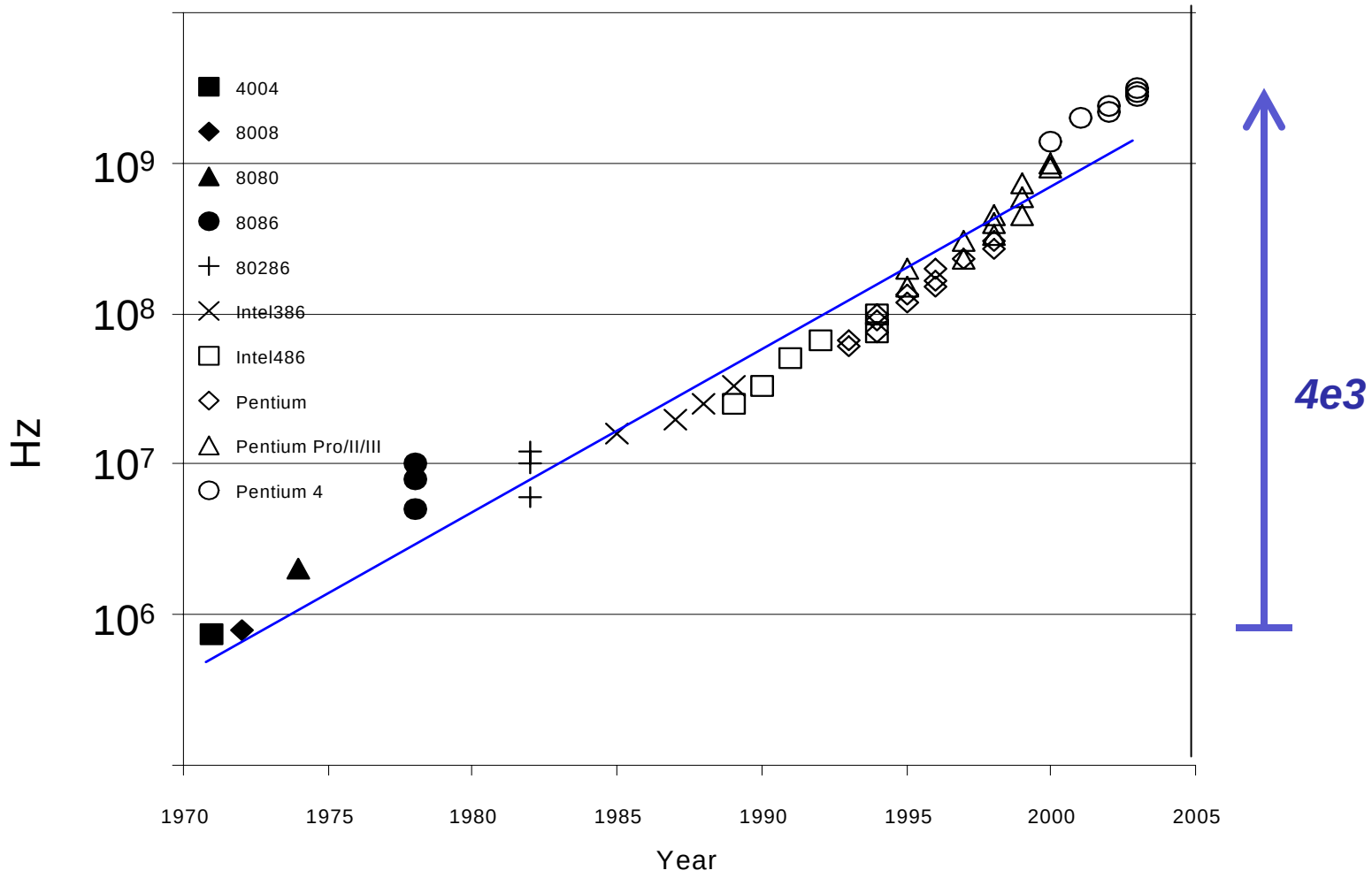
- New generation every ~2 years with $\alpha = \sqrt{2}$
- L_g (1970) 8 μm (2007) 18 nm



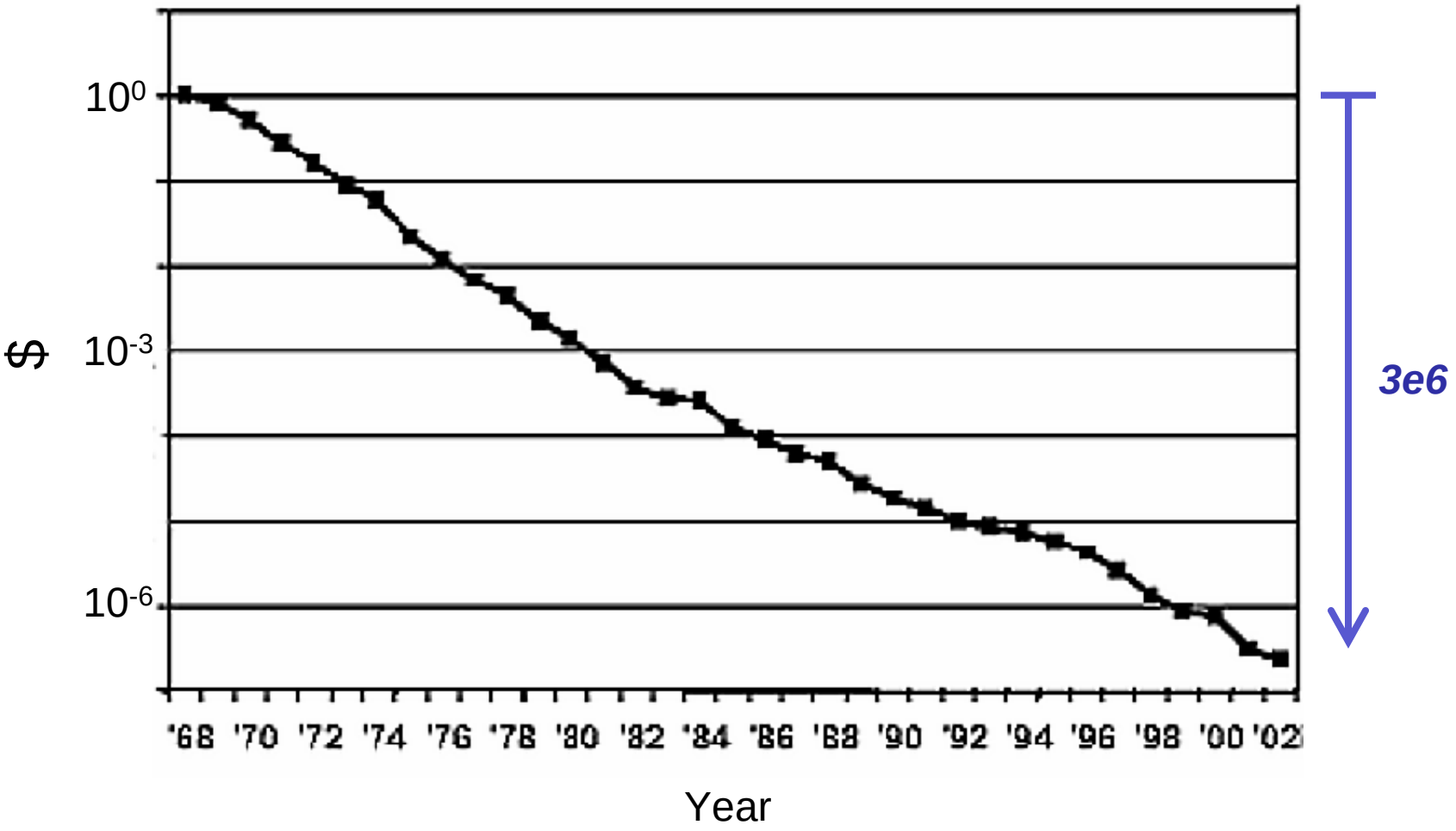
Transistor Count



CPU Clock Frequency

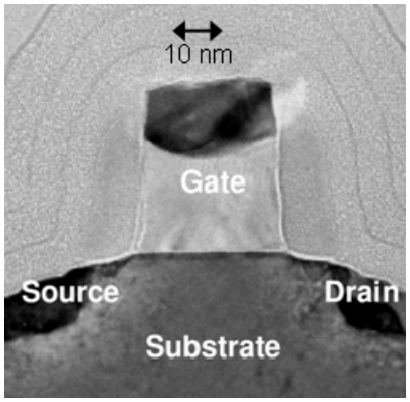


Transistor Cost

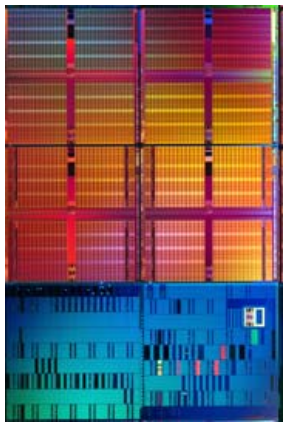


Digital State of the Art

- 65 nm node:
  - SRAM test chip Nov. 2003
  - production Nov. 2005
  - “crossover” 3Q 2006



- 45 nm node:
  - 153MB SRAM Jan. 2006
  - >10^9 MOSFETs
  - production 3Q ‘07



Failures of Classical Scaling

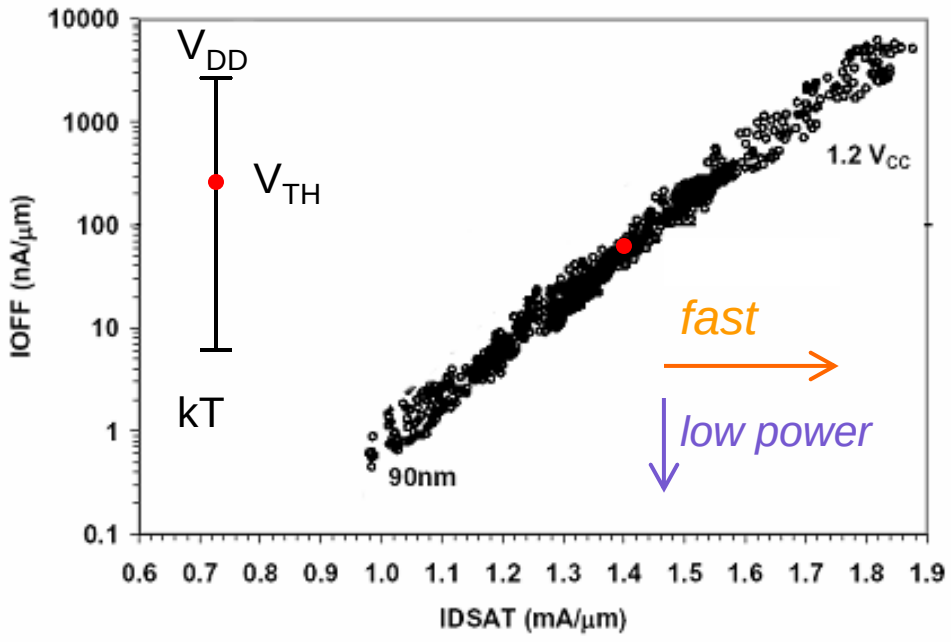
- ignores kT
- ignores mobility degradation and velocity saturation
- ignores fringing capacitance
- ignores tunneling
- ignores atomistic effects
- ignores industry economics

kT ≠ 0

- MOSFET in weak inversion when $V_{gs} < V_{th}$:

$$I_D = I_0 e^{\frac{q(V_{GS} - V_{TH})}{nkT}} \Rightarrow I_{off} = I_0 e^{\frac{-qV_{TH}}{nkT}}$$

- Can't continue to scale V_{TH}
- Tradeoff of speed for leakage current (static power)
- Multi-V_{TH} processes

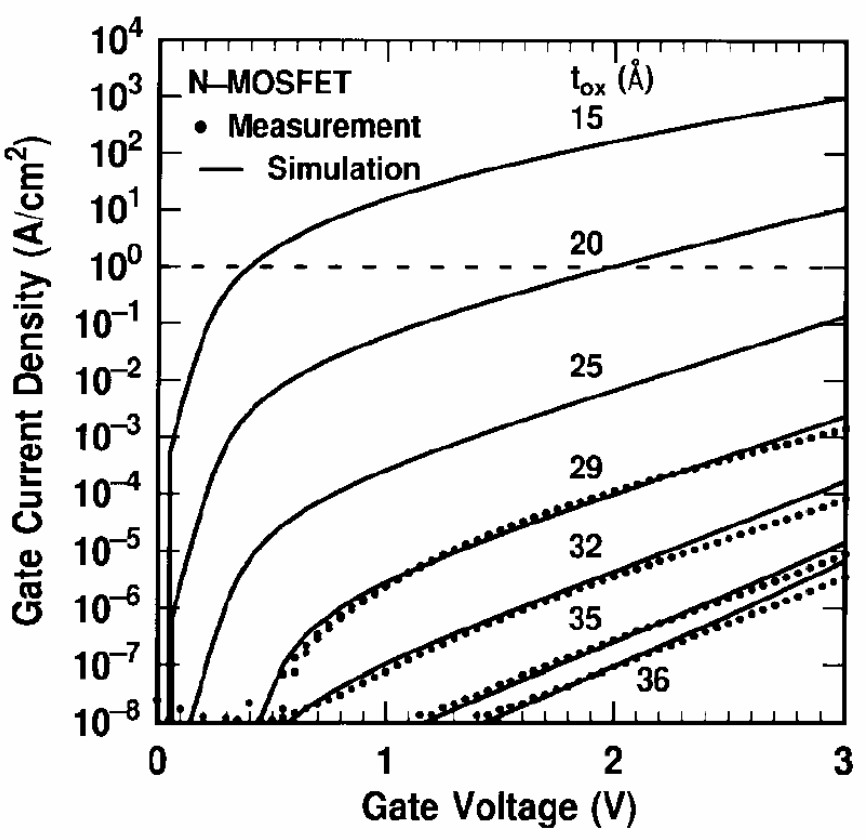


Gate tunneling current

- Significant tunneling through SiO_2 when t_{ox} < 3nm
- J_{tunnel} increases 100X per generation
- Replace SiO_2 with high-κ dielectric (?)

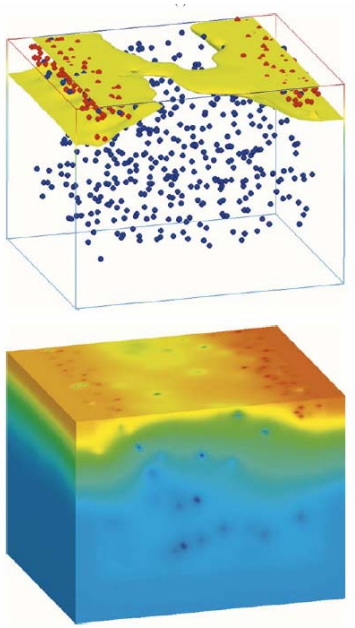
$$EOT = t_{hi-\kappa}\frac{\varepsilon_{SiO_2}}{\varepsilon_{hi-\kappa}}$$

- Multi-t_{ox} processes



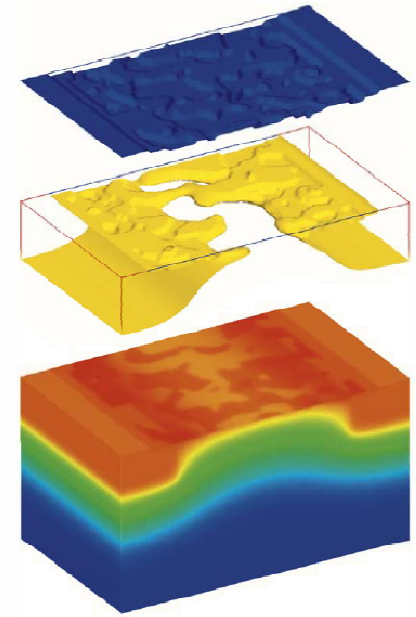
Atomistic Effects

random dopant distribution



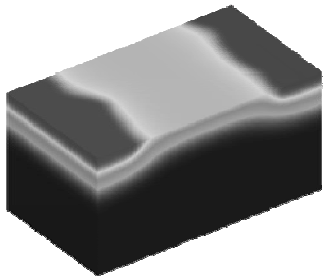
σV_{TH}, RTS

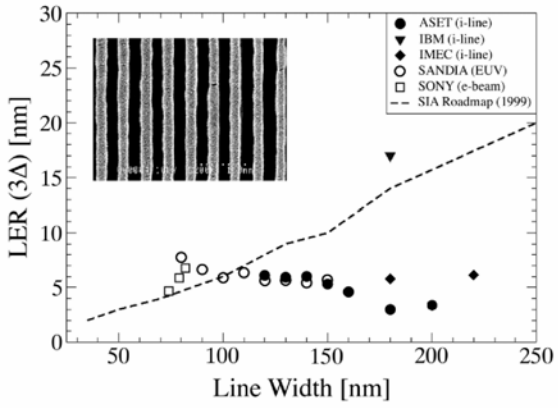
oxide thickness variation



σV_{TH}, σJ_{tunnel}, $\sigma \mu$

line edge roughness



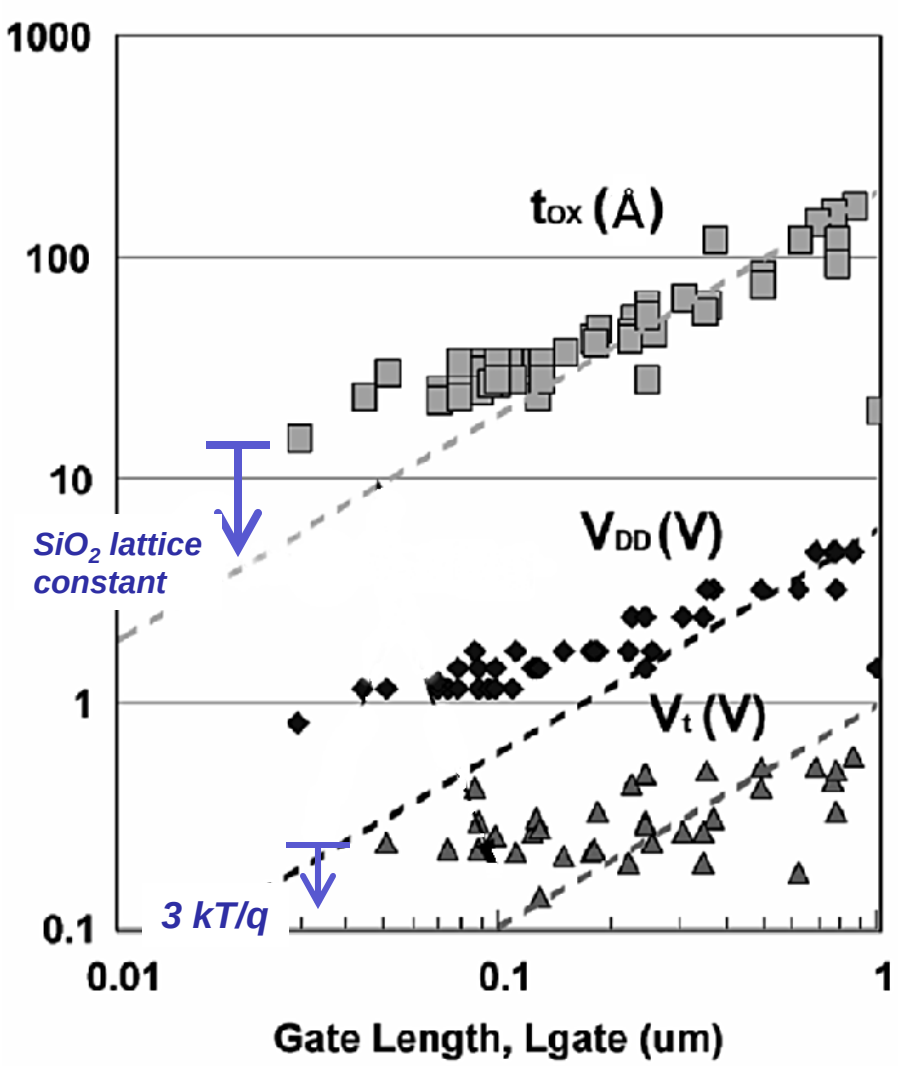


σV_{TH}

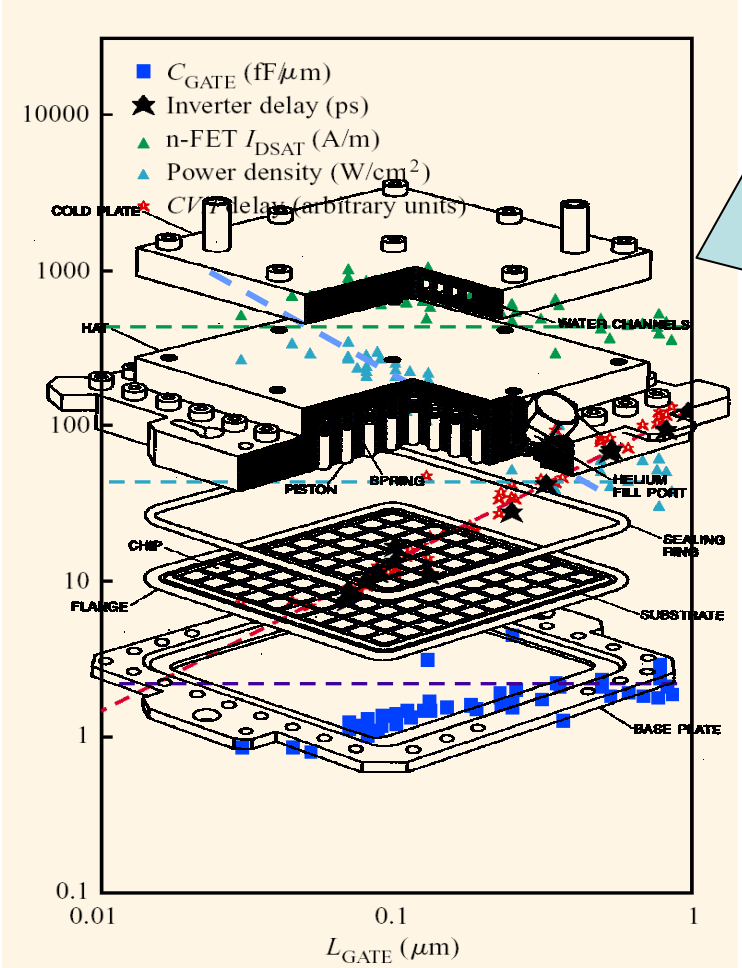
A. Asenov, IEEE Trans. Electron Dev. 50(9), 1837 (2003)

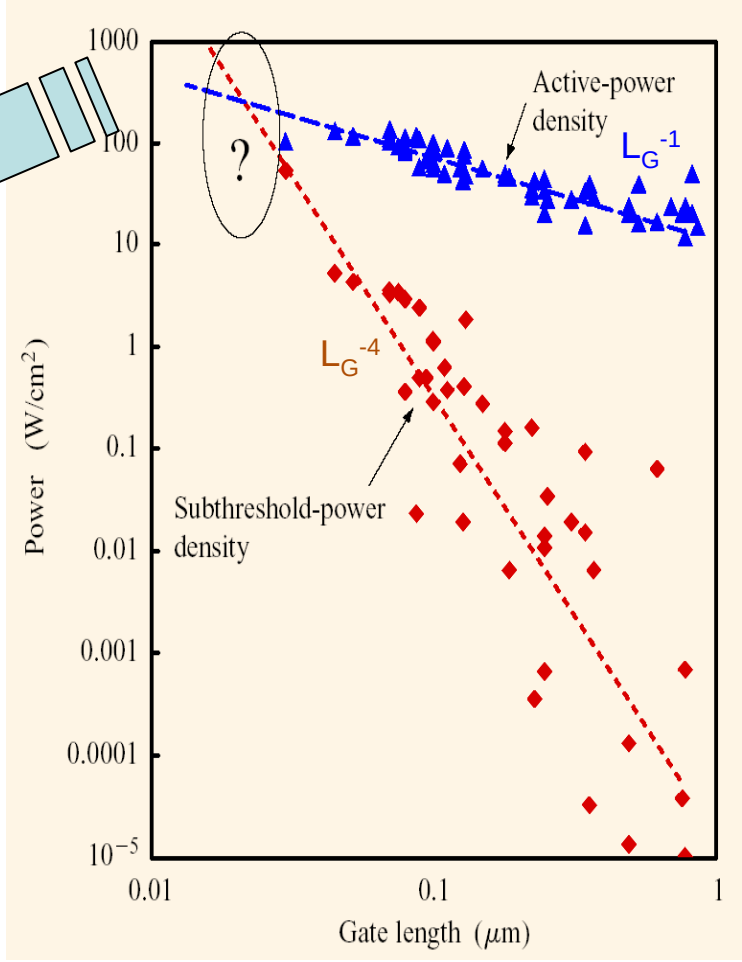
Scaling in Practice

- Until 180nm node:
  - follow classical scaling with $\alpha = \sqrt{2}$
  - *2.8X performance per generation*
- Now:
  - continue (super) scaling L_g
  - sub-scaling of t_{ox}
  - V_{DD}, V_{TH} have stopped scaling
- Gate density and speed continue to scale
- Increase of E, conductance
- Switching energy decreases only by $1/\alpha$ not $1/\alpha^3$
- Power density *increase* ~ α
- Static power from leakage, gate tunneling make power problem worse



Power is biggest impediment to further scaling



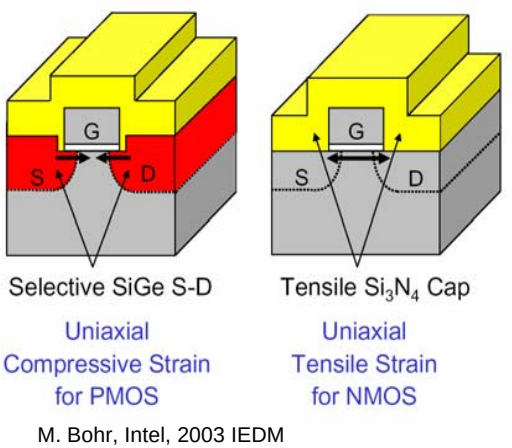


E. Nowak, IBM J. Res. & Dev. 45(2), 169 (2002)

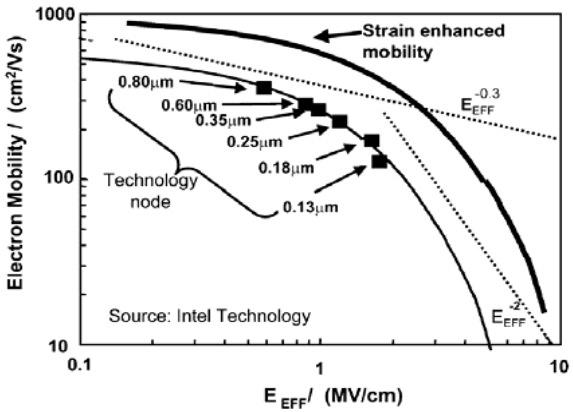
Next-generation Transistors

Strain Engineering

- *Reduce mobility degradation*



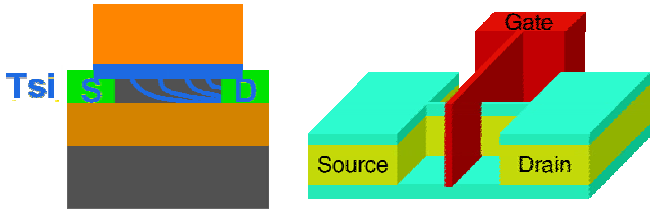
M. Bohr, Intel, 2003 IEDM

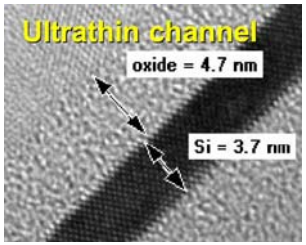


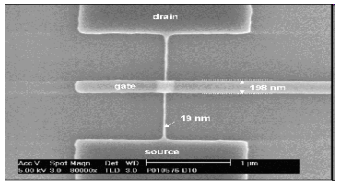
S. Thompson, Intel,IEEE T-ED 51(11), 1790 (2004)

UTSOI, DG-FET

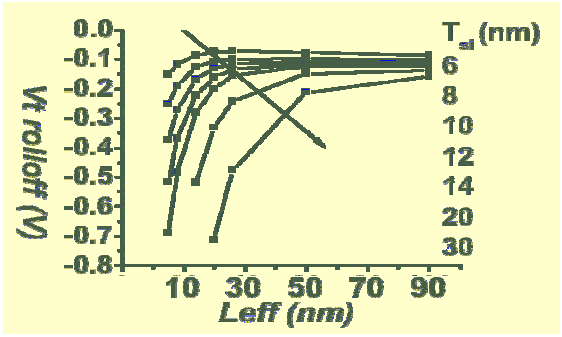
- *Suppress SCE through improved electrostatics*







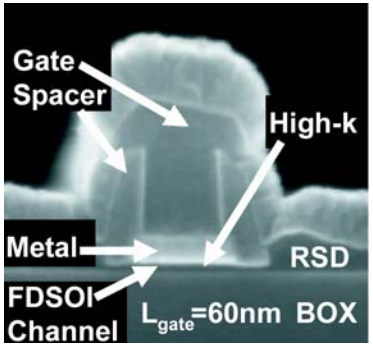
F.-L. Yang et al., IMEC, 200 VLSI Symp.

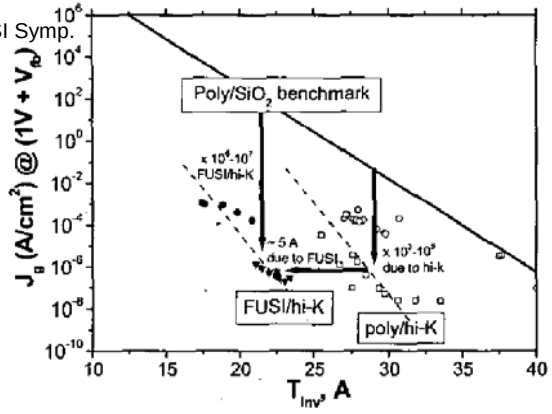


M. Ieong, IBM, Sol. State and IC Tech. 2004

High-k gate dielectric

- *Suppress J_{tunnel}*

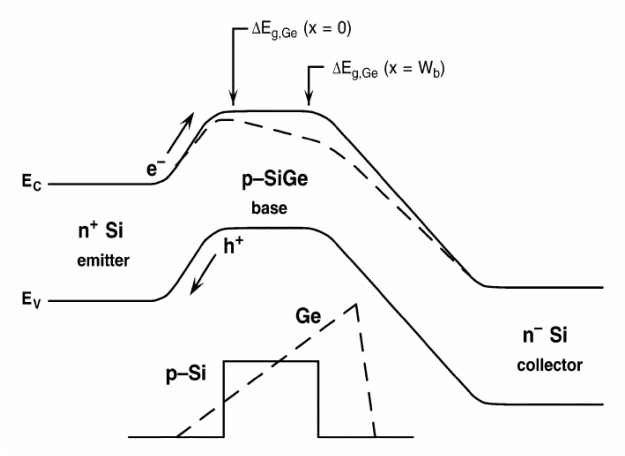


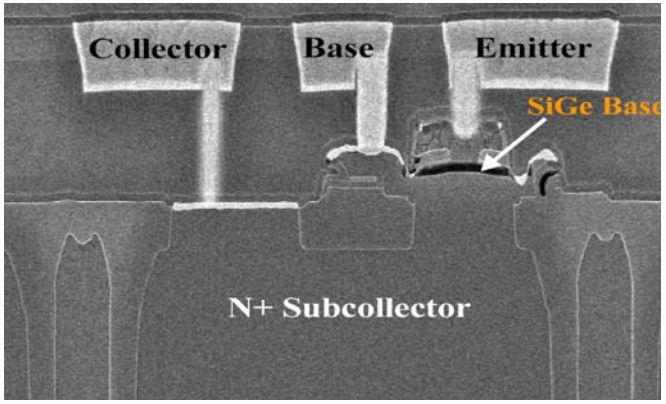


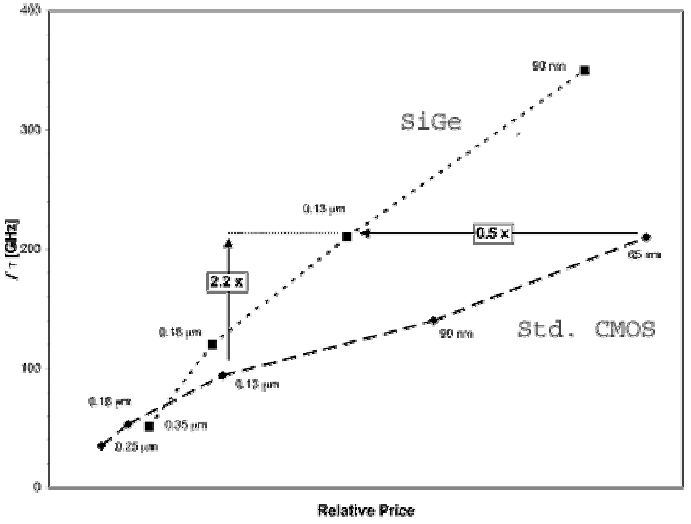
E. Gusev et al., IBM, 2004 IEDM

SiGe Heterojunction Bipolar Transistor (HBT)

- Power-performance ~ 2X standard CMOS at same feature size
- Cost also ~ 2X
- Provides 3 – 4 year “head start” over CMOS
- Eventually CMOS provides better cost-performance

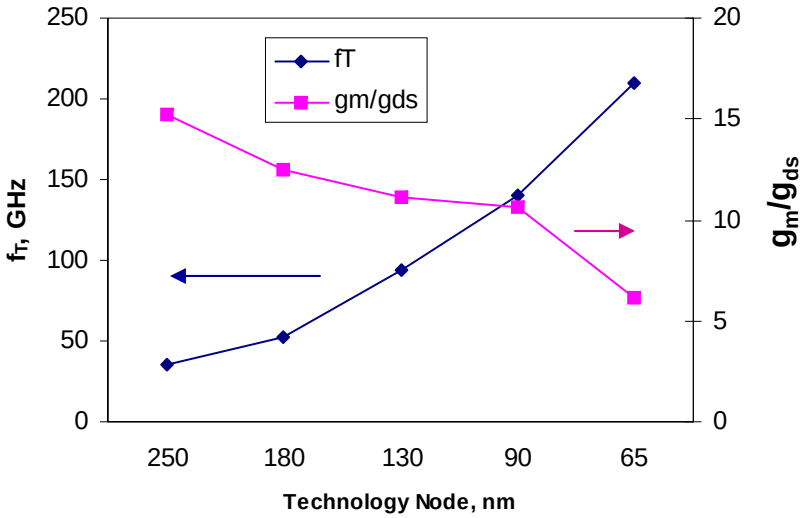


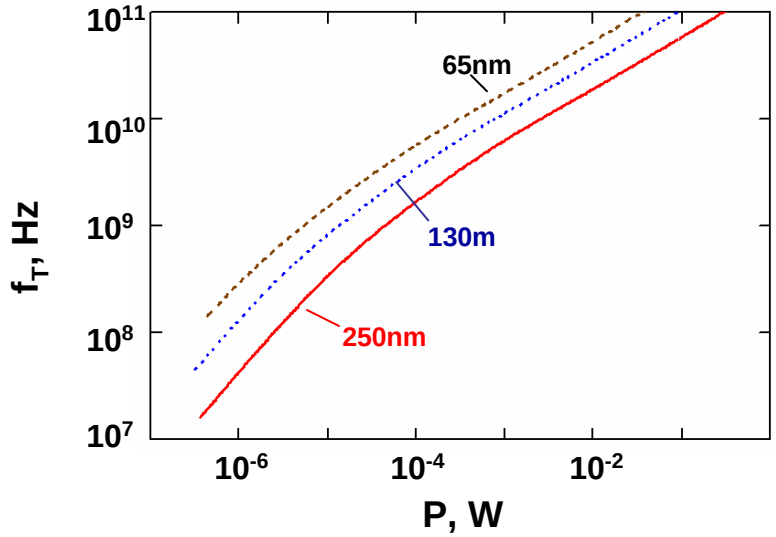


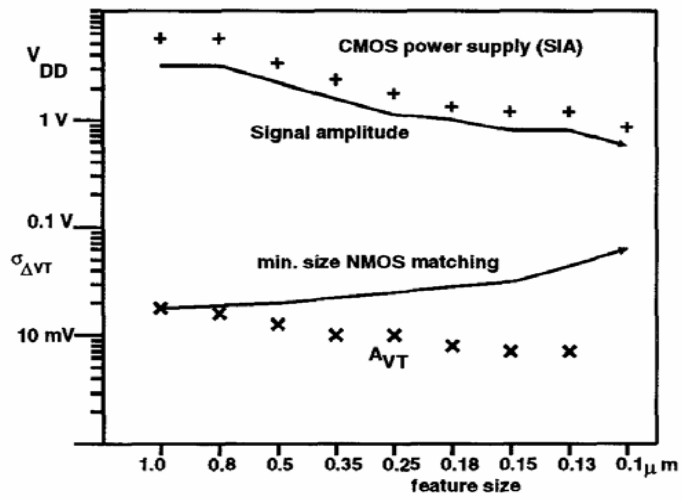


Analog: Speed, Gain & Matching

- Speed/intrinsic gain tradeoff
  - $f_T \sim 1/L_G$ for min-L_G devices
  - Output conductance g_{ds} sensitive to geometry and bias
  - Gain g_m/g_{ds} severely degraded in ultra-scaled devices:
    - failure to adhere to classical constant-E scaling
- Threshold Mismatch
  - Dopant fluctuations: $\sigma_{\Delta VTH,LG-\min} \sim \alpha$
  - Overcome by increasing W*L
  - Power penalty



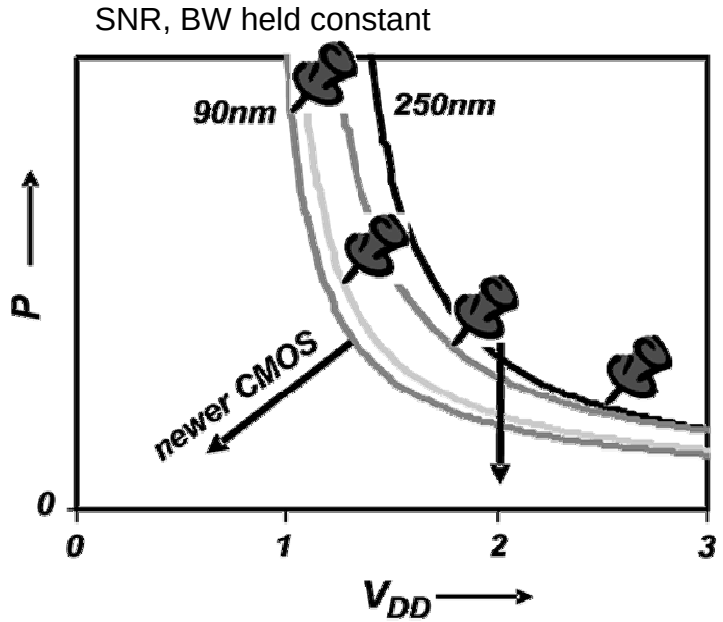




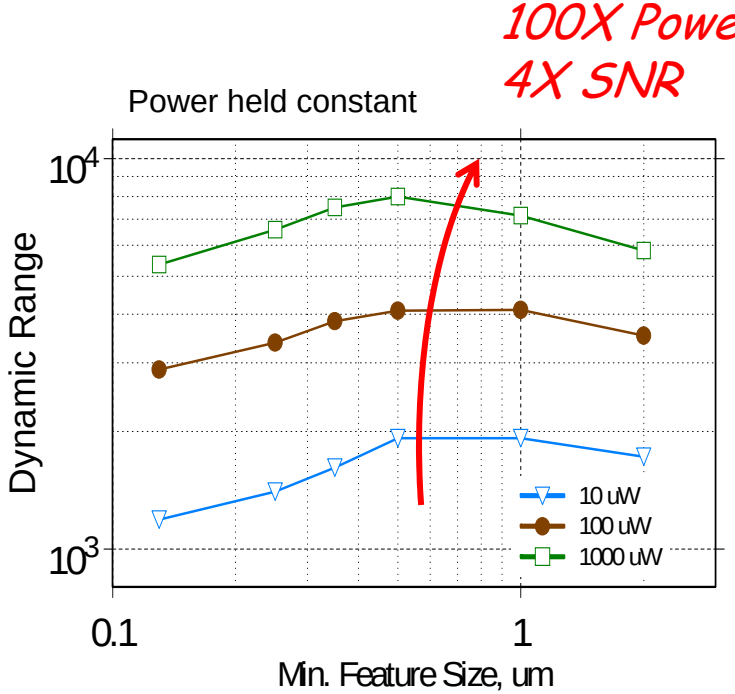
Pelgrom, Philips, 1998 IEDM

Analog Low-V_{DD} Challenges

- Increasing ratio of V_{TH}/V_{DD} rules out use of many classical analog design toplogies, e.g. cascodes.
- To achieve same performance at lower V_{DD}, analog circuits need *increased* power.



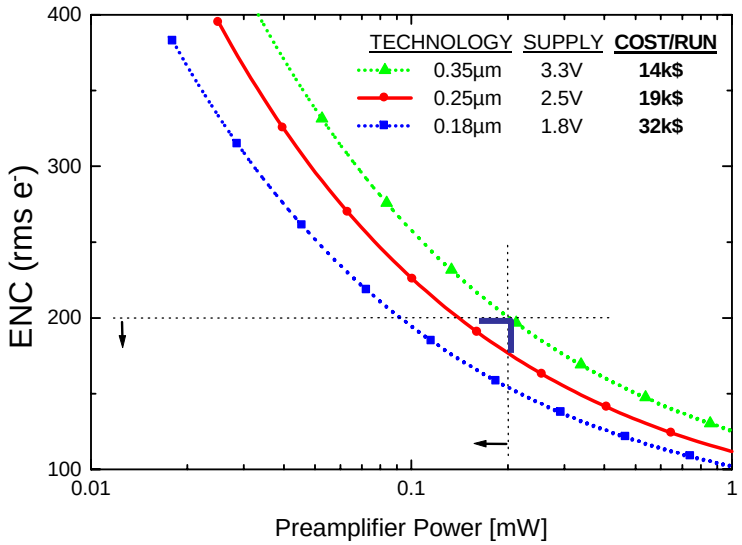
(performance limited by thermal noise)



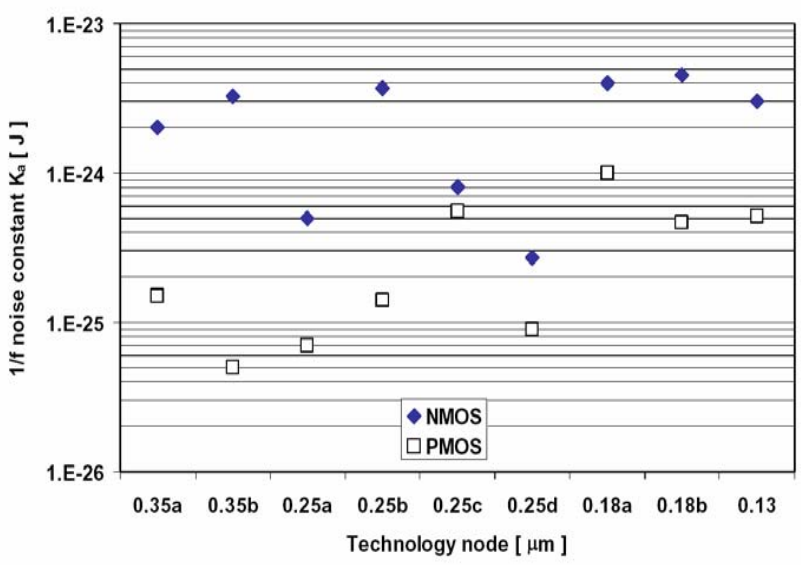
A. Annema et al., IEEE JSSS 40(1), 132 (2005)

Noise in scaled CMOS

- For CSA, consider noise in relation to gate capacitance
- Thermal noise improvement from higher f_T:
  - $ENC_{th} \sim \sqrt{1/\alpha}$
- 1/f noise depends on interface trap density, device area, inversion charge density –
  - no consistent trend with scaling
- Choice of L,W for minimum noise needs to account for moderate inversion operation
- Gate leakage current shot noise (parallel)



P O'Connor and G. De Geronimo, Prospects for charge sensitive amplifiers in scaled CMOS, NIM A480, 713 (Mar. 2002)

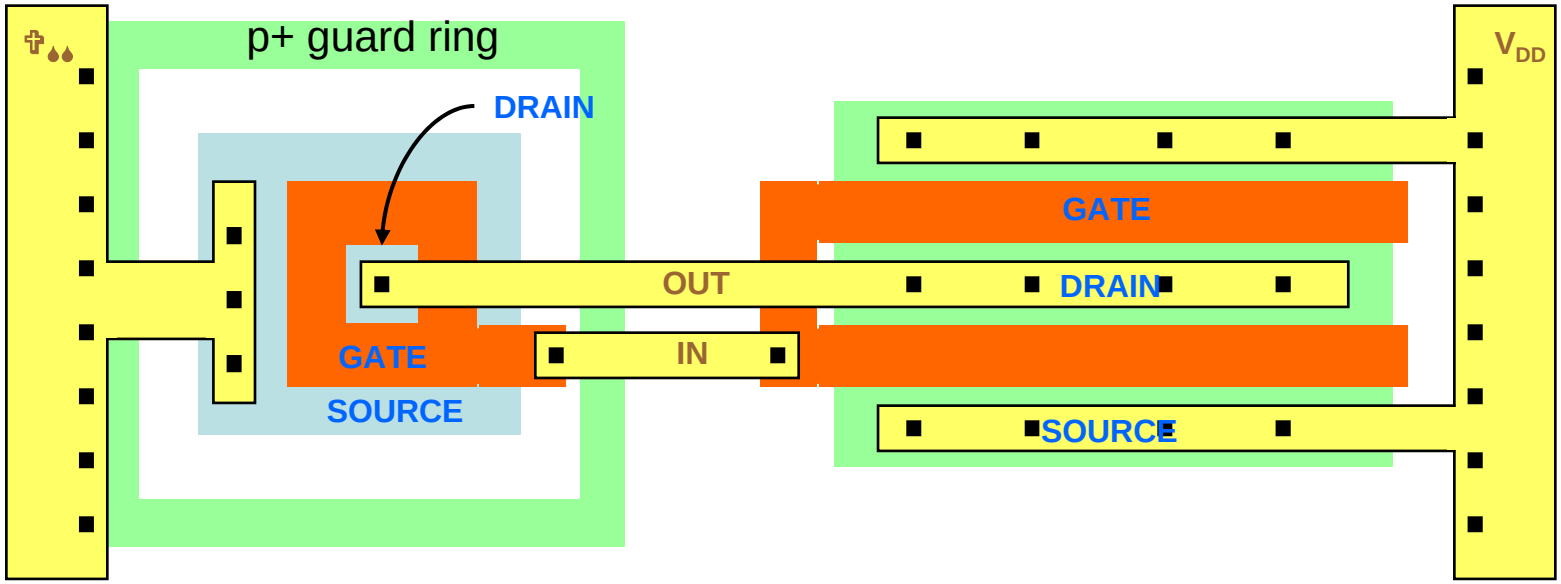


G. Anelli 2005

Radiation Tolerant Inverter

NMOS Enclosed Layout Transistor (ELT)

PMOS



metal 1

polysilicon

n+ diffusion

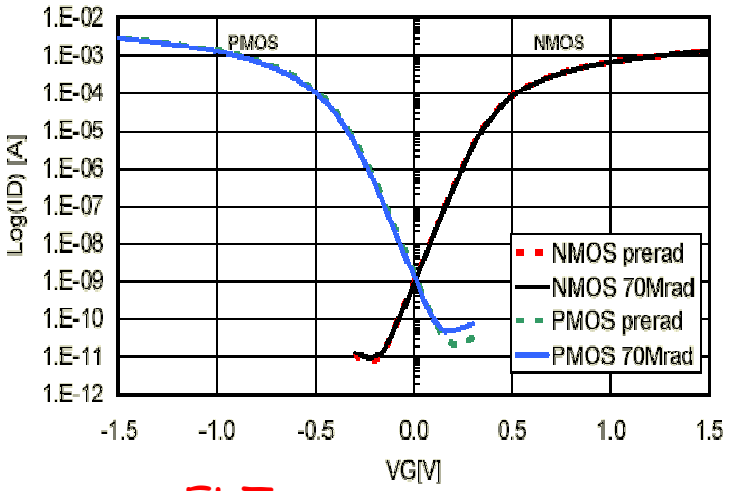
p+ diffusion

contact to diffusion

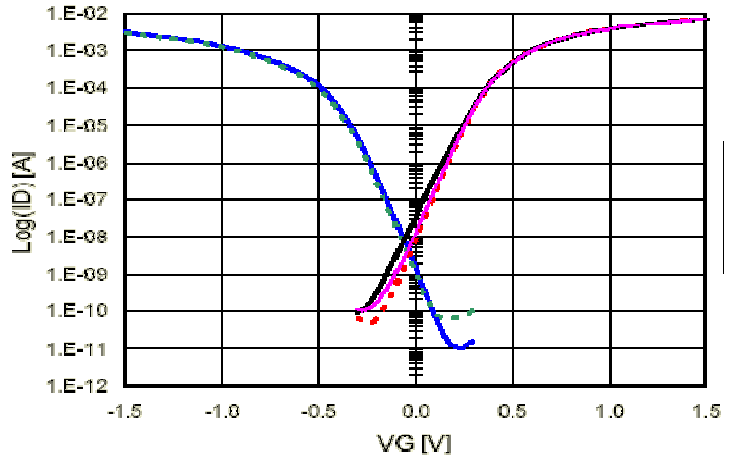
Radiation Effects below 0.25μm

- Thinner gate oxides ➔ more tolerance to Total Ionizing Dose
- Thick field oxide charging ➔
  - edge leakage in NMOS
  - loss of isolation NWELL-NWELL
- 0.13μm IBM technology harder than 0.25μm:
  - non-ELT devices OK except narrow/thick-oxide NMOS
  - to 70 Mrad+
  - lateral isolation OK, no guard ring needed
  - SEU cross section higher, lower critical charge
  - No radiation-induced SEL

ELT

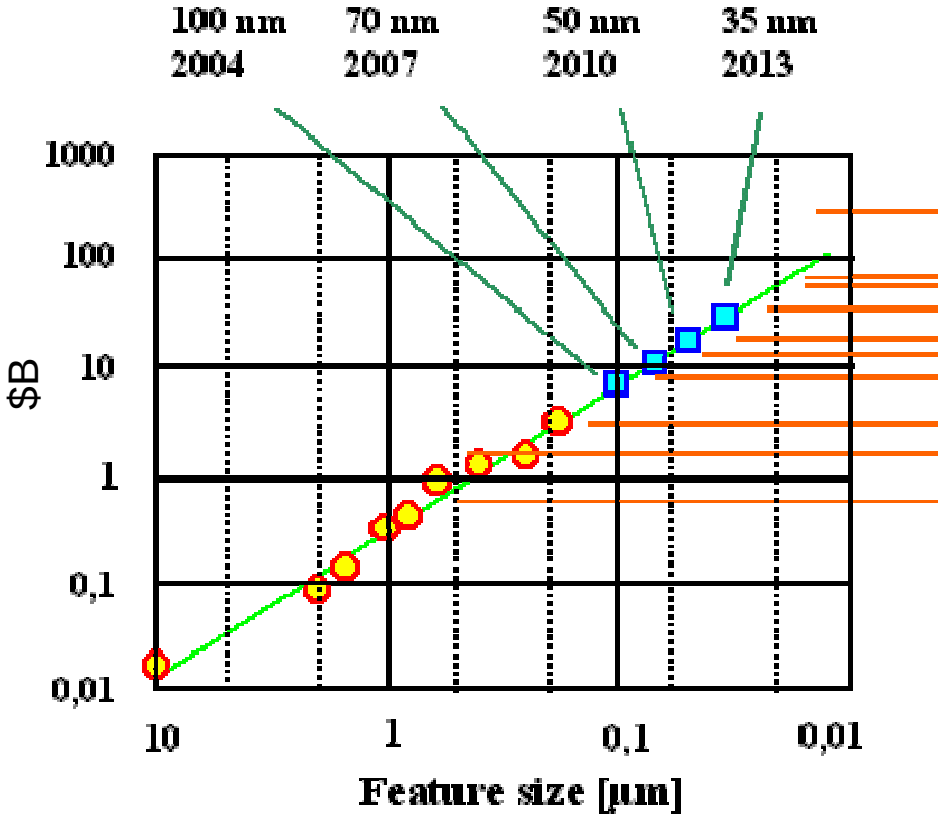


non-ELT



F. Faccio, CERN, FEE Workshop Snowmass 2003

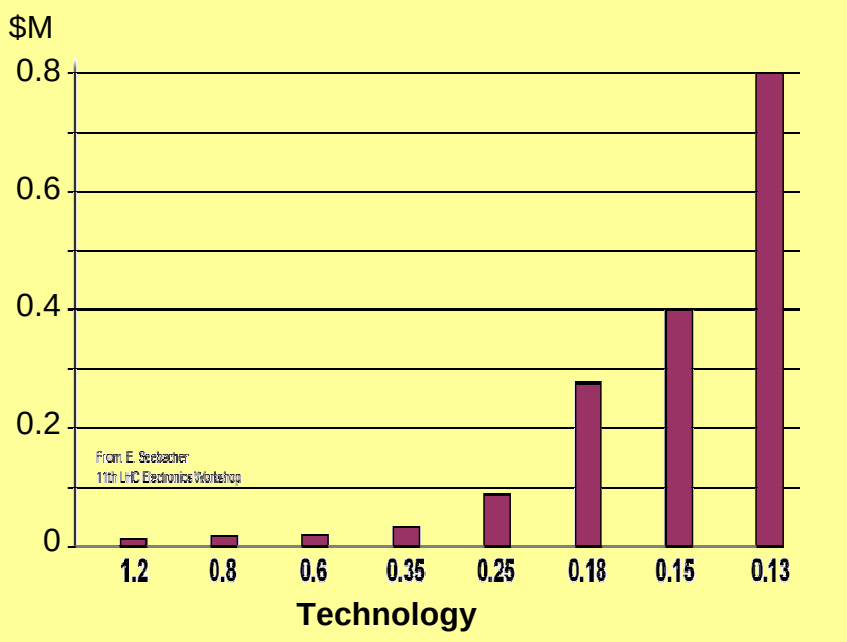
Fab Line Cost



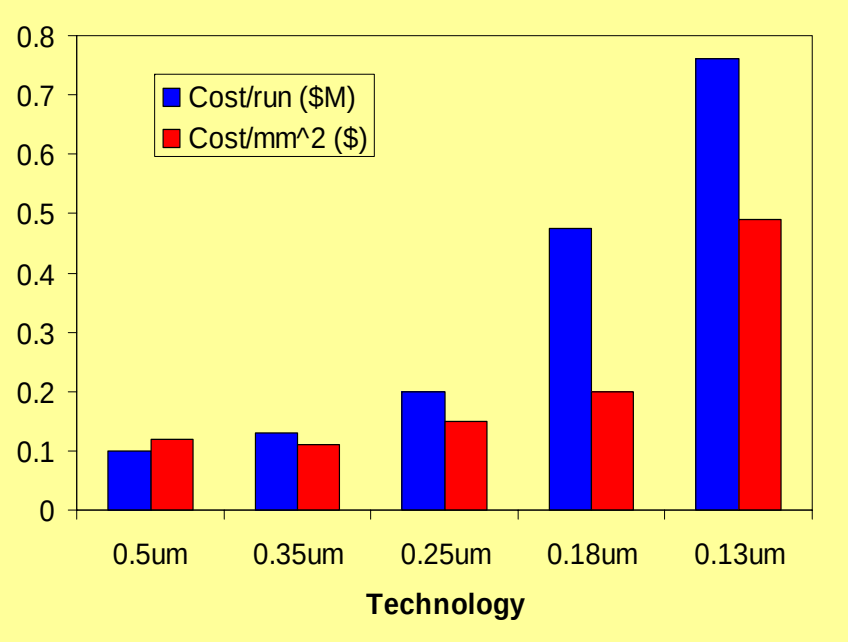
http://www.tf.uni-kiel.de/matwis/amat/elmat_en/index.html
Electronic Materials
© Prof. Dr. Helmut Föll
University of Kiel; Faculty of Engineering

Mask Set and Fabrication Cost

MASK SET



ENGINEERING RUN



Example - BNL ASIC Design Group

- Develops Low Noise FEE for gas and semiconductor detectors
  - accelerator experiments
  - medical imaging
  - astrophysics
  - homeland security
- 70% Federal, 30% commercial
- Staff
  - 5 ASIC professionals
  - 1 DAQ engineer
  - 1 Technician
- CAD suite and test labs
- 7 – 8 runs/year through MOSIS
  - 0.35, 0.25, and 0.18um mixed-signal CMOS
  - 5K – 600K MOSFETs per chip
  - $20K – $80K per MPW run
- Development cost per design ~ *$200K x no. revisions needed*

Summary

- Power dissipation is the major obstacle to further CMOS scaling.
- Foundry and mask costs going up as process options (multi-V_{th}, multi-t_{ox}, HBT, passives, etc.) added for SOC.
- Analog design is compromised by the low supply rail.
- Except for high radiation resistance and packing density, ultra-scaled technologies offer few advantages to justify their enormous cost.
- Plenty of opportunity to innovate in (n-4)-generation CMOS.

Bon Appétit!